Trainer Module: ETEK ECS-6500-03

Chapter Five

DPSK Modulator

ETEK TECHNOLOGY CO., LTD.

E-mail: etek21@ms59.hinet.net

http: // www.etek21.com.tw

5-1 Curriculum Objectives

1. To understand the theory of DPSK modulation.
2. To understand the signal waveform of DPSK encoder.
3. To design the DPSK modulator by using MC1496.
4. To understand the methods of measuring and adjusting the DPSK modulation circuit.

5-2 Curriculum Theory

In communication system, besides PSK modulation that we have mentioned before, there is another type of modulation, which we called differential phase shift keying (DPSK) modulation. Both PSK and DPSK modulations use the variation of phase of the carrier to modulate the data signal. In phase modulation, the amplitude and frequency remain the same; the only difference is the phase.

Generally speaking, the transmission velocity of the increasingly data rate will consume more bandwidths; PSK modulation conceals the modulated signals in phase, so PSK modulation will not have this phenomenon.

The phase difference of the carrier of the PSK modulated signal is 180° that represents “0” or “1” for the data signal in figure 5-1(a). The DPSK modulation signal will transmit 1-bit signal in figure 5-1(b). Both DPSK and PSK modulations use data signals in same type.

(a) PSK vector diagram (b) DPSK vector diagram

Figure 5-1 Vector diagram of PSK and DPSK.

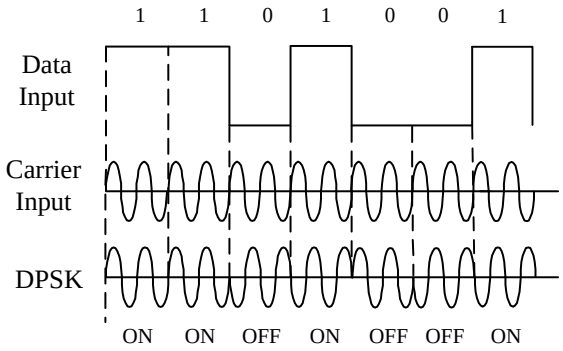


Figure 5-2 DPSK modulation signal waveforms.

The electric circuit of DPSK modulator is mainly made of two electric circuits: The first circuit is called the differential encoder circuit, its function mainly is to code the data of the input. The other one is called phase shift keying (PSK) circuit, its function is mainly to modulate the data after being coded and the carry signal. The DPSK modulation signal waveforms are made of two ways to show the digital data and are shown in figure 5-2. If the data signal is 0-bit that is the phase shift of the modulated signal is 180° out of phase. If the data signal is 1-bit, that is the phase shift of the modulated signal is 0° out of phase. Receiver needs to have the capability of the storage, the talent of the exactitude decoding the data of reception.

According to the characteristic of DPSK encoder, we can get its equation of coding shown as equation 5-1. The C_k is shown as differential encoded sequence. D_k is shown as input data bit. The output waveforms of DPSK encoder are shown as figure 5-2.

1. If the data signal is 1-bit, the output data of differential encoder (C_k) is same as the carry signal is 0° out of phase.

2. If the data signal is 0-bit, the output data of differential encoder (C_k) is opposite as the carry signal is 180° out of phase.

$$C_k = \overline{D_k \oplus C_{k-1}} \qquad (5\text{-}1)$$

The above equation also can be expressed as

$$D_k = \overline{C_k \oplus C_{k-1}} \qquad (5\text{-}2)$$

We can use equation 5-2 to design the DPSK encoder and it is shown in Fig. 5-3. The pseudo data generator in diagram is mainly to generate a virtual data. The second and third stages of flip-flop will latch up input data. If the output signal of XNOR gate is C_k, the second stage output signal of flip-flop is D_k, and then, the third stage output signal of is C_{k-1}. Usage the data of the second and third stages of flip-flop input to XNOR, we will get the output data of DPSK encoder.

The binary signal is used to shift the phase between 0° and 180°, which is called phase shift keying (PSK) modulation.

M-ary PSK can be expressed as

$$x_{PSK}(t) = A\cos[\omega_c t + (2m-1)\frac{\pi}{M}]\ ;\quad m = 1, \cdots, M \qquad (5\text{-}3)$$

If the data signal is 1-bit, that is M = 2. So, $x_{PSK}(t)$ will transmit binary bits signal and the phase shift of the modulated signal is 180° out of phase. Equation 5-3 shows the signal waveform of binary phase shift keying, (BPSK). The BPSK signal at logic 1 is represented as $A\cos(\omega_c t + \pi/2)$ and the BPSK signal at logic 0 is represented as $A\cos(\omega_c t + 3\pi/2)$.

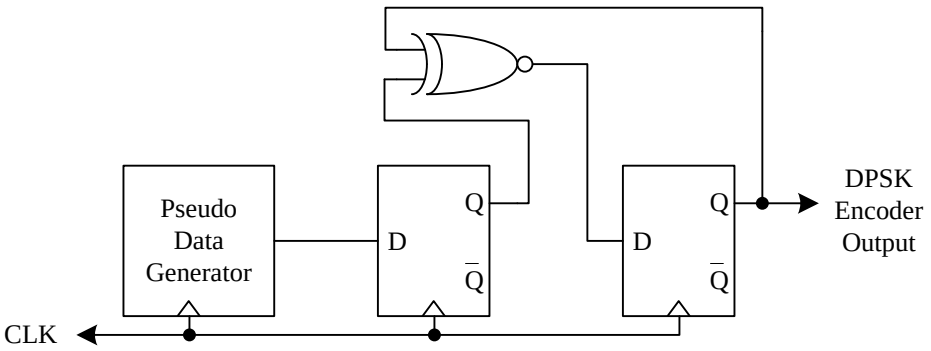


Figure 5-3 Circuit diagram of DPSK digital encoder.

Figure 5-4 is the basic block diagram of DPSK modulator, which the DPSK modulator must make the digital signals input to the product encoder, and let the signal pass through a unipolar/bipolar converter, then, at the output port, we can obtain the bipolar data signal. Finally, let the bipolar data signal and carry signal pass through the balanced modulator which can meet the objectives of phase modulation, and the bandpass filter will remove the unwanted frequency signals to make the DPSK signal waveform perfectly.

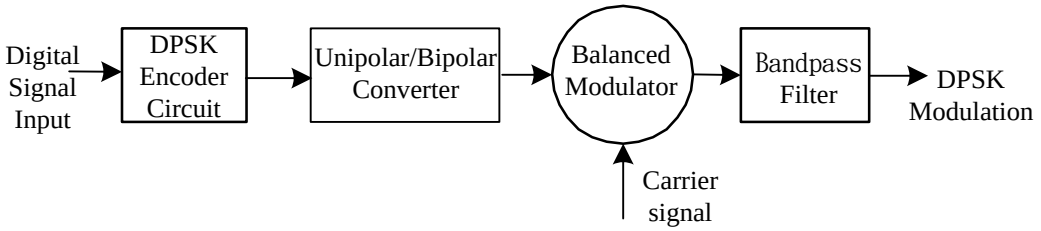


Figure 5-4 Basic block diagram of DPSK modulator.

In this experiment, MC1496 is used to implement the balanced modulator. Figure 5-5 is the internal circuit diagram of MC1496. From the circuit diagram, D_1, R_1, R_2, R_3, Q_7 and Q_8 comprise the current source, which provides Q_5 and Q_6 with DC bias current. Q_5 and Q_6 comprise the differential transistor, which is used to drive the Q_1, Q_2, Q_3 and Q_4 that is the dual differential amplifiers.

Pin 1 and pin 4 are for data signal input. Pin 8 and pin 10 are for carrier signal inputs. The gain of balanced modulator is controlled by the external resistor between pin 2 and pin 3. The bias voltage of the amplifier can be determined by the external resistor connected at pin 5.

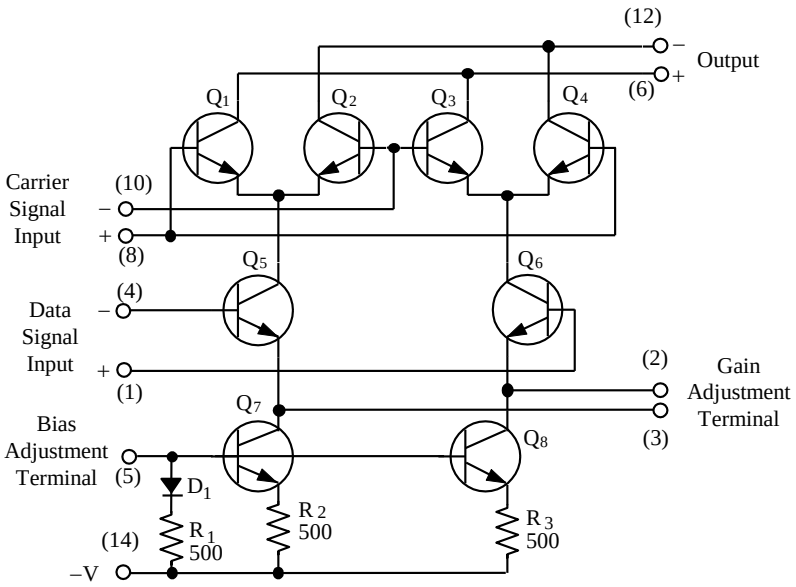


Figure 5-5 Internal circuit diagram of MC1496.

Figure 5-6 is the circuit diagram of 2-bit PSK which the carrier signal and data signal are single-ended input. Pin 10 is the carrier input and the data signal is passed through the unipolar to bipolar converter which is comprised by 74HCU04, 74HC126, 3904, 3906, D_1, D_2, D_3 and R_1 to R_8. The converted bipolar signal will be sent to pin 1 of MC1496. R_{22} determines the gain of the circuit and R_{23} determines the bias voltage of the circuit. If we adjust VR_1 or change the amplitude of the data signal, then we can prevent the PSK modulation signal from distortion. This signal will be sent to the filter, which is comprised by μA741, C_4, C_6, R_{26}, R_{27} and R_{28}. Then the unwanted frequency signals which are produced by the balanced modulator will be filtered and a better DPSK signal will be performed.

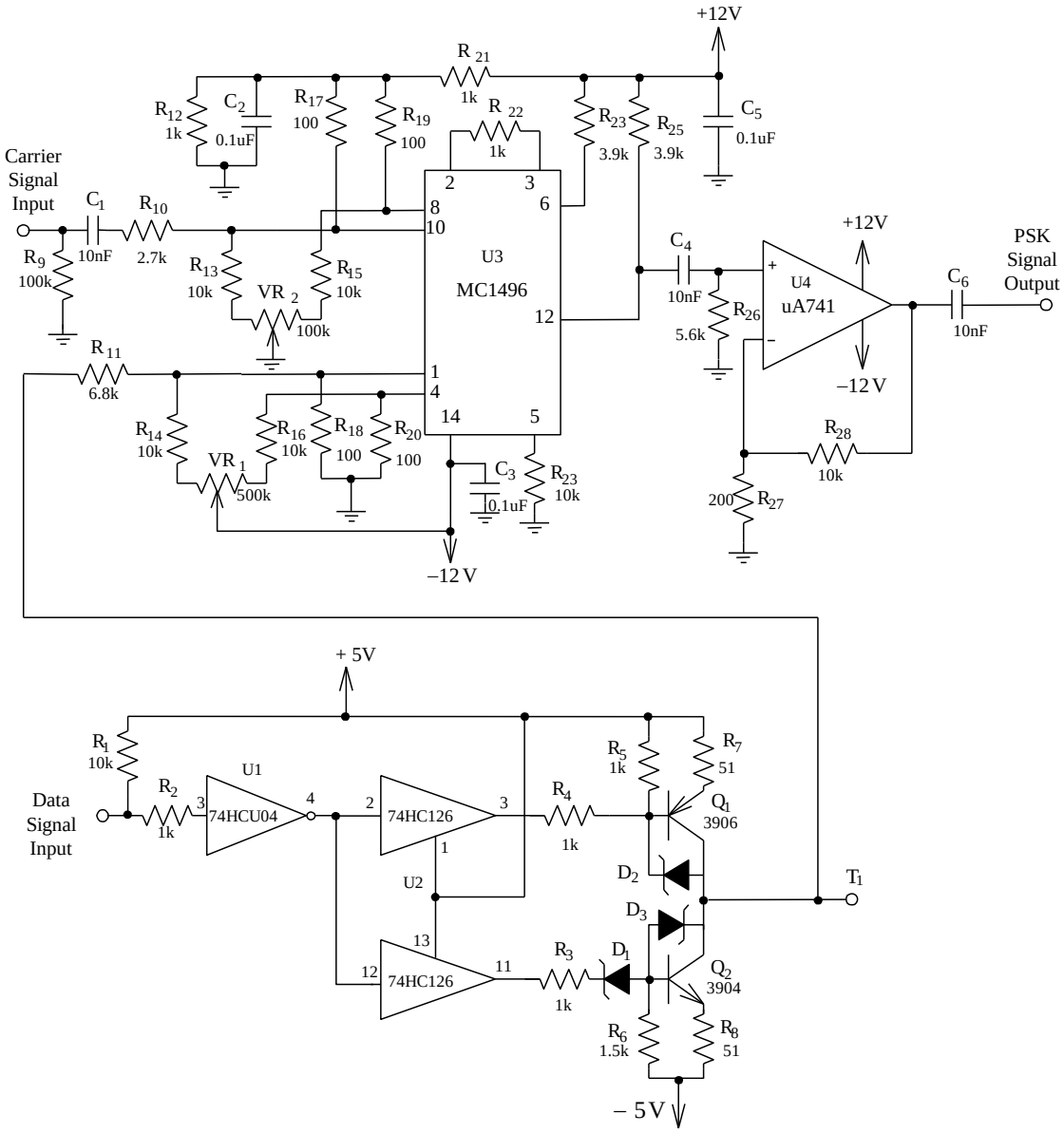


Figure 5-6 Circuit diagram of DPSK modulator by using MC1496.

5-3 Experiment Items

Experiment 1: DPSK Encoder

1. Refer to the circuit diagram in figure 5-3 or figure ECS5-1 on ETEK ECS-6500-03 module.
2. At the input port (CLK I/P) of clock signal, input 5 V amplitude and 200 Hz square wave frequency with 50 % duty cycle (that is, using TTL signal).
3. By using oscilloscope, observe at the output port (Data) of the pseudo data generator and the output port (TP1) of DPSK encoder. Record the measured results in table 5-1.
4. At the input port (CLK I/P) of clock signal, input 5 V amplitude and 300 Hz square wave frequency with 50 % duty cycle (that is, using TTL signal).
5. By using oscilloscope, observe at the output port (Data) of the pseudo data generator and the output port (TP1) of DPSK encoder. Record the measured results in table 5-1.
6. At the input port (CLK I/P) of clock signal, input 5 V amplitude and 400 Hz square wave frequency with 50 % duty cycle (that is, using TTL signal).
7. By using oscilloscope, observe at the output port (Data) of the pseudo data generator and the output port (TP1) of DPSK encoder. Record the measured results in table 5-1.

Experiment 2: DPSK Modulator

1. Refer to the circuit diagram in figure 5-6 or figure ECS5-1 on ETEK ECS-6500-03 module.

2. At the input port (CLK I/P) of clock signal, input 5 V amplitude and 200 Hz square wave frequency with 50 % duty cycle (that is, using TTL signal).

3. At the input port (Carrier I/P) of carrier signal, input 600 mV amplitude and 20 kHz waveform.

4. By using oscilloscope, observe at the output waveform of DPSK modulator (DPSK O/P). After that adjust variable resistor “Carrier Adjuster” until the waveform does not appear distortion and also slightly adjust variable resistor “Data Adjuster” to reduce the asymmetry of the waveforms.

5. By using oscilloscope, observe on the output terminal (Data) of the pseudo data generator and the output port (TP1) of DPSK encoder, the test point (TP2) of carrier signal, the output port (TP3) of bipolar/unipolar converter, the output port (TP4) of balanced modulator, and the output port (DPSK O/P) of DPSK signal. Record the measured results in table 5-2.

6. At the input port (Carrier I/P) of carrier signal, input 600 mV amplitude and 50 kHz waveform.

7. By using oscilloscope, observe at the output waveform of DPSK modulator (DPSK O/P). After that adjust variable resistor “Carrier Adjuster” until the waveform does not appear distortion and also slightly adjust variable resistor “Data Adjuster” to reduce the asymmetry of the waveforms.

8. By using oscilloscope, observe on the output terminal (Data) of the pseudo data generator and the output port (TP1) of DPSK encoder, the test point (TP2) of carrier signal, the output port (TP3) of bipolar/unipolar converter, the output port (TP4) of balanced modulator, and the output port (DPSK O/P) of DPSK signal. Record the measured results in table 5-2.

9. At the input port (Carrier I/P) of carrier signal, input 600 mV amplitude and 80 kHz waveform.

10. By using oscilloscope, observe at the output waveform of DPSK modulator (DPSK O/P). After that adjust variable resistor “Carrier Adjuster” until the waveform does not appear distortion and also slightly adjust variable resistor “Data Adjuster” to reduce the asymmetry of the waveforms.

11. By using oscilloscope, observe on the output terminal (Data) of the pseudo data generator and the output port (TP1) of DPSK encoder, the test point (TP2) of carrier signal, the output port (TP3) of bipolar/unipolar converter, the output port (TP4) of balanced modulator, and the output port (DPSK O/P) of DPSK signal. Record the measured results in table 5-2.

12. At the input port (CLK I/P) of clock signal, input 5 V amplitude and 200 Hz square wave frequency with 50 % duty cycle (that is, using TTL signal).

13. At the input port (Carrier I/P) of carrier signal, input 800 mV amplitude and 20 kHz waveform.

14. By using oscilloscope, observe at the output waveform of DPSK modulator (DPSK O/P). After that adjust variable resistor “Carrier Adjuster” until the waveform does not appear distortion and also slightly adjust variable resistor “Data Adjuster” to reduce the asymmetry of the waveforms.

15. By using oscilloscope, observe on the output terminal (Data) of the pseudo data generator and the output port (TP1) of DPSK encoder, the test point (TP2) of carrier signal, the output port (TP3) of bipolar/unipolar converter, the output port (TP4) of balanced modulator, and the output port (DPSK O/P) of DPSK signal. Record the measured results in table 5-3.

16. At the input port (Carrier I/P) of carrier signal, input 1.2 V amplitude and 20 kHz waveform.

17. By using oscilloscope, observe at the output waveform of DPSK modulator (DPSK O/P). After that adjust variable resistor “Carrier Adjuster” until the waveform does not appear distortion and also slightly adjust variable resistor “Data Adjuster” to reduce the asymmetry of the waveforms.

18. By using oscilloscope, observe on the output terminal (Data) of the pseudo data generator and the output port (TP1) of DPSK encoder, the test point (TP2) of

carrier signal, the output port (TP3) of bipolar/unipolar converter, the output port (TP4) of balanced modulator, and the output port (DPSK O/P) of DPSK signal. Record the measured results in table 5-3.

5-4 Experimental Results

Experiment 1: DPSK Encoder

Table 5-1 Measured results of pseudo data and encoder signal

Clock Signal Frequency	Data	TP1
TTL @ 200 Hz		
TTL @ 300 Hz		
TTL @ 400 Hz		

Experiment 2: DPSK Modulator

Table 5-2 Measured results of DPSK modulation
($V_C = 600\ mV_{PP}$, $f_{CLK} = 200\ Hz$)

Carrier Signal Frequency	Carrier I/P	Data
20 kHz		
	TP1	TP2
	TP3	TP4
	DPSK O/P	

Table 5-2 Measured results of DPSK modulation (cont.)
($V_C = 600\ mV_{PP}$, $f_{CLK} = 200\ Hz$)

Carrier Signal Frequency	Carrier I/P	Data
50 kHz		
	TP1	TP2
	TP3	TP4
	DPSK O/P	

Table 5-2 Measured results of DPSK modulation (cont.)
($V_C = 600\ mV_{PP}$, $f_{CLK} = 200\ Hz$)

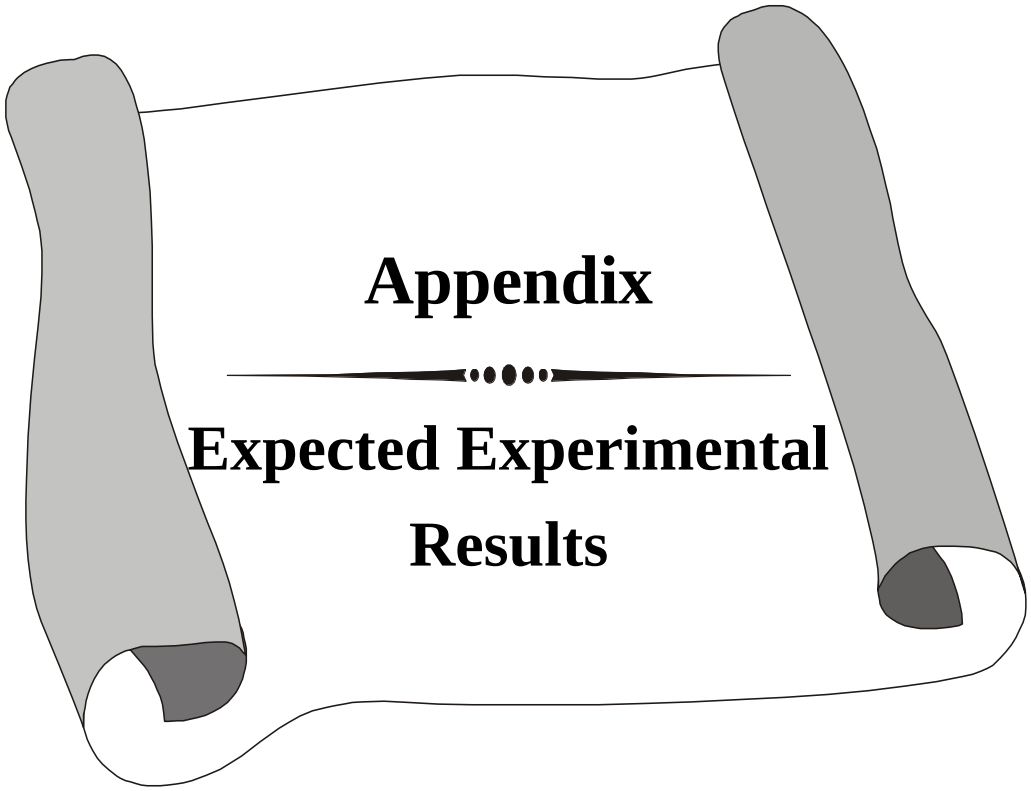
Carrier Signal Frequency	Carrier I/P	Data
80 kHz		
	TP1	TP2
	TP3	TP4
	DPSK O/P	

Table 5-3 Measured results of DPSK modulation
($f_C = 20$ kHz, $f_{CLK} = 200$ Hz)

Carrier Signal Amplitude	Carrier I/P	Data
800 mVpp		
	TP1	TP2
	TP3	TP4
	DPSK O/P	

Table 5-3 Measured results of DPSK modulation (cont.)
($f_C = 20$ kHz, $f_{CLK} = 200$ Hz)

Carrier Signal Amplitude	Carrier I/P	Data
1.2 V_{pp}		
	TP1	TP2
	TP3	TP4
	DPSK O/P	



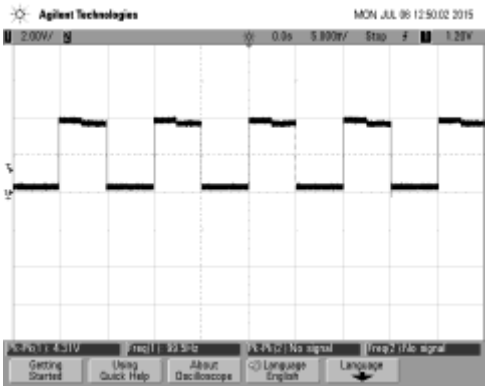
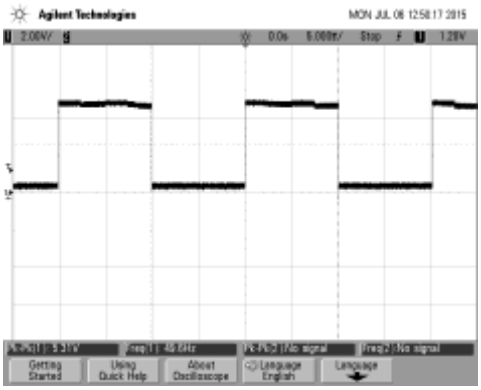
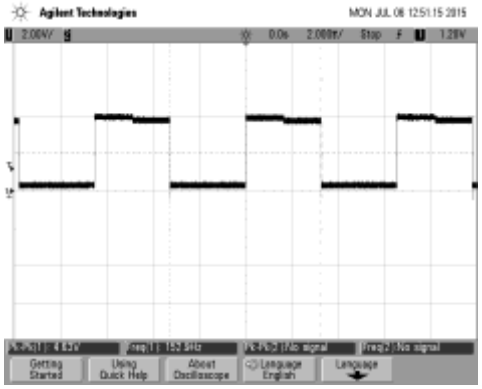
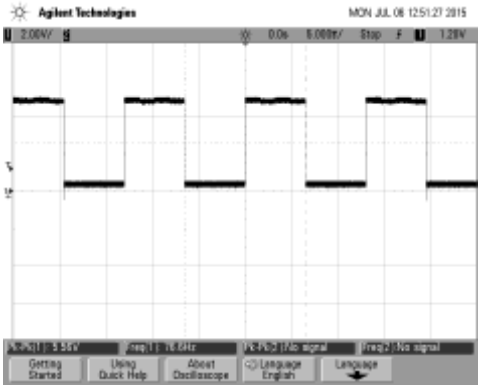
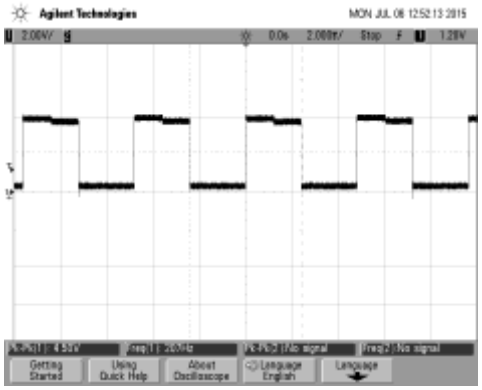
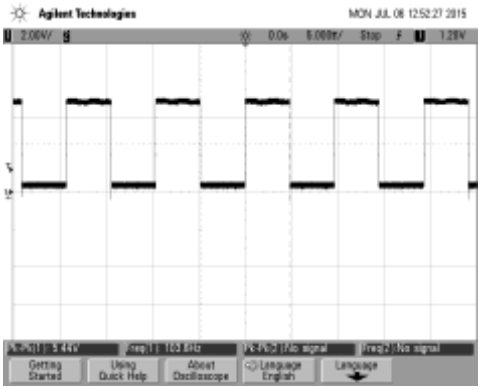
Appendix

Expected Experimental Results

Chapter 5 Expected Experimental Results

Experiment 1: DPSK Encoder

Table 5-1 Measured results of pseudo data and encoder signal

Clock Signal Frequency	Data	TP1
TTL @ 200 Hz		
TTL @ 300 Hz		
TTL @ 400 Hz		

Experiment 2: DPSK Modulator

Table 5-2 Measured results of DPSK modulation
($V_C = 600\ mV_{PP}$, $f_{CLK} = 200\ Hz$)

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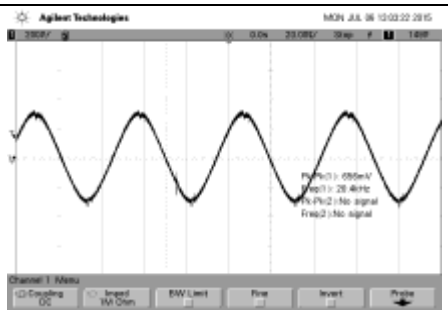
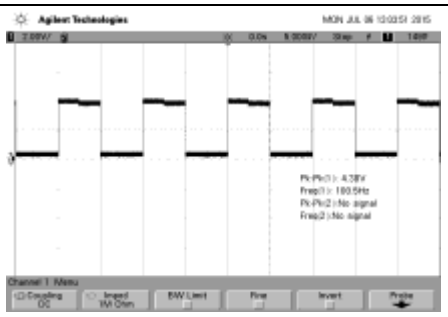
<tr><td>  </td><td>  </td></tr>
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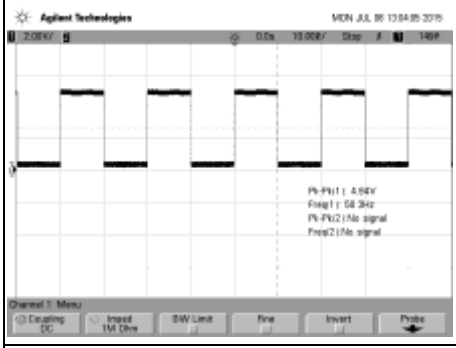
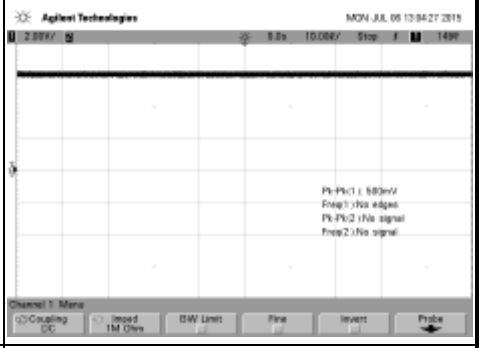
<tr><td>  </td><td>  </td></tr>
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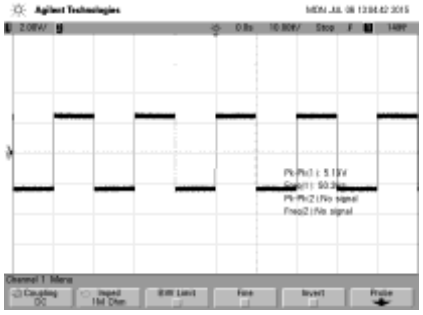
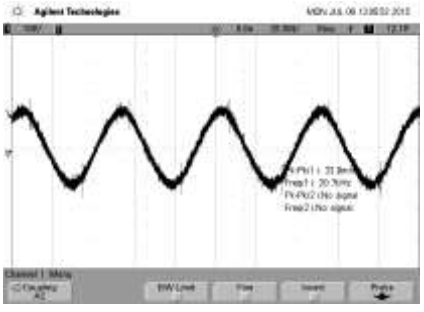
<tr><td>  </td><td>  </td></tr>
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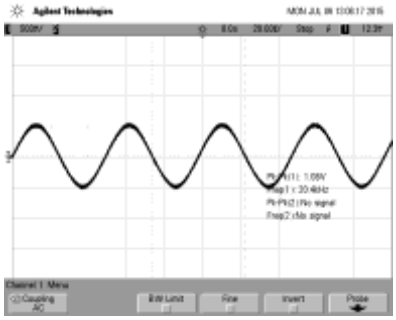
<tr><td colspan="2">  </td></tr>
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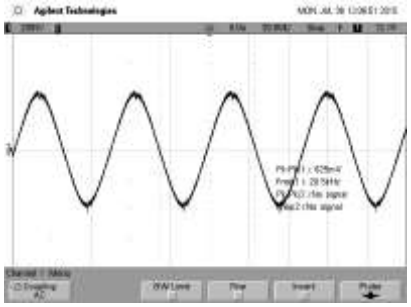
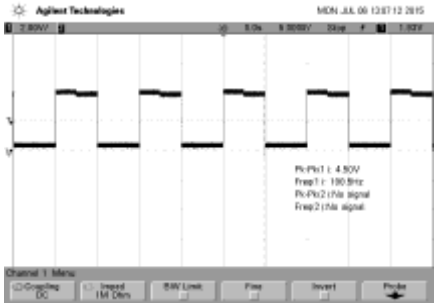
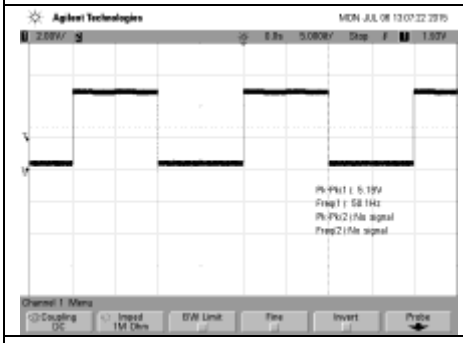
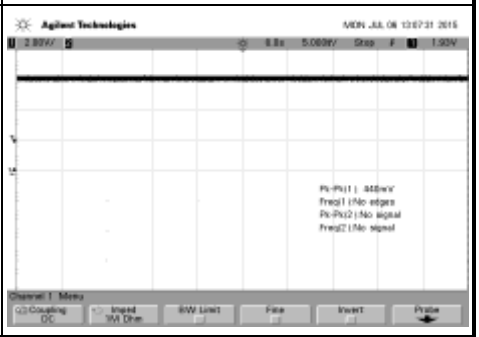
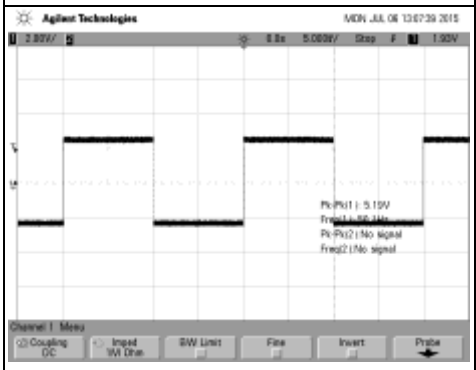
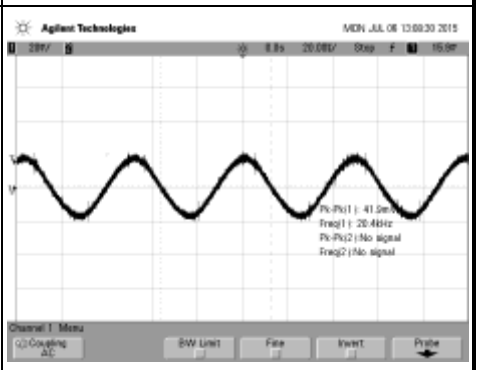
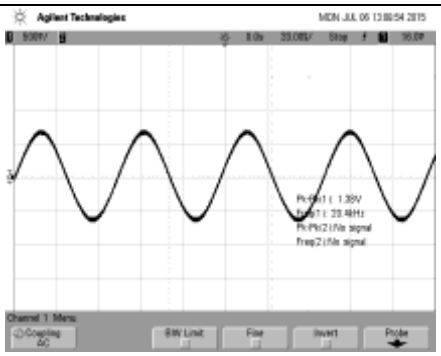
Table 5-3 Measured results of DPSK modulation
($f_C = 20\ \ kHz,\ \ f_{CLK} = 200\ \ Hz$)

Carrier Signal Amplitude	Carrier I/P	Data
800 mVpp		
	TP1	TP2
		
	TP3	TP4
		
	DPSK O/P