Trainer Module: ETEK MSA-2003-04

Chapter Six

Phase Locked Loop Controller

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I. Curriculum Objectives

1. To understand the applications of 89C51 microcontroller.
2. To implement a phase locked loop (PLL) controller by using 89C51 microcontroller.
3. To understand the theory and applications of the interrupted and uninterrupted keypad scanning circuit.
4. To understand the applications of liquid crystal display (LCD) and the implementation of LCD interface.

II. Curriculum Theory

In order to operate PLL frequency synthesizer, we must implement a controller to control the PLL frequency synthesizer. Therefore we will introduce the applications of 89C51 microcontroller in this chapter. Besides 89C51, the entire controller includes a keypad circuit and LCD. The operation items are keyed in from keypad and display on LCD. Thus, it will be easier for the operation of interface and the selection of frequency. On the other hand, the keypad interface can be handled by an interrupted mode or uninterrupted mode. For interrupted mode, if no command from keypad, microcontroller does not need to scan the keypad. At this time microcontroller can be used at other applications such as information processing or diversity controlling. This type of interface is easy to expand to other external devices, but must use complicated external interrupt trigger and scanning circuit. For uninterrupted mode, the circuit structure is simple and unnecessary to use an external processing circuit, but the program will become more complicated and not easy for expansion. In the processing of the circuit design, we will leave some spaces includes the output and input ports (I/O Port), the technological process of the programming, and so on. So that it will be easy for us to expand the system in future.

6-1 The Hardware Structure of Controller

Figure 6-1 is the block diagram of controller with interrupted mode keypad interface. The block diagram includes 89C51 microcontroller, keypad, keypad scanning circuit and LCD. We can key in the operation items or data from keypad and observe the input values or operation items on LCD. After that produce the control signal via 89C51 and send the related values to MB 15E03L PLL frequency synthesizer. As for uninterrupted mode keypad interface, then from figure 6-1, the keypad can directly connect to 89C51 without adding keypad scanning circuit as shown in figure 6-2.

6-1-1 The Planning for I/O Ports of 89C51 Microcontroller

The functions of 89C51 microcontroller are quite complete and it works as a microcontroller, which is being used popularly in other applications. 89C51 microcontroller includes I/O interface, interrupt, clock, programmable memory and RAM. With these functions, the circuit design become simple and does not need to consider the clock problem between each chip. The planning for I/O ports of 89C51 microcontroller is shown in table 6-1. From the planning in table 6-1, the microcontroller can communicate with other peripherals.

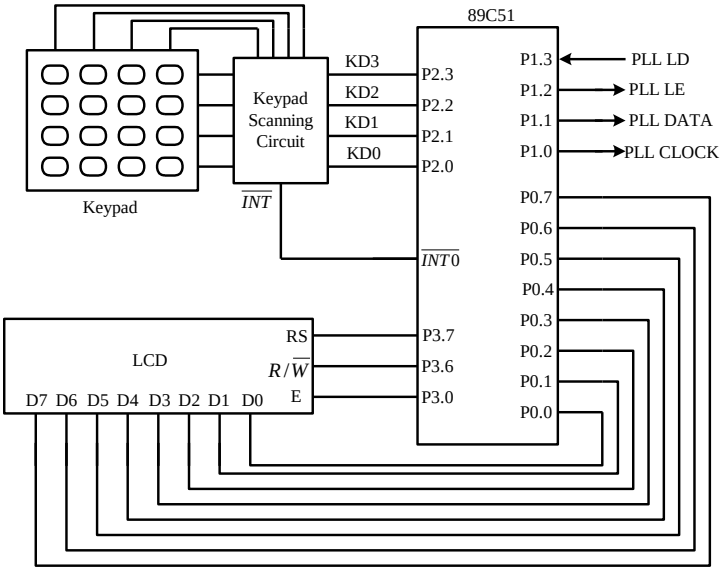


Figure 6-1 Block diagram of controller with interrupted mode keypad interface.

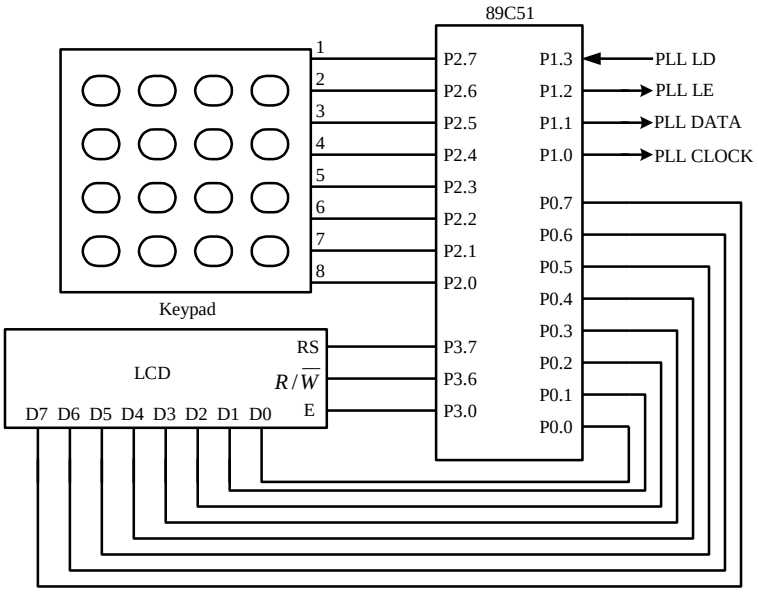
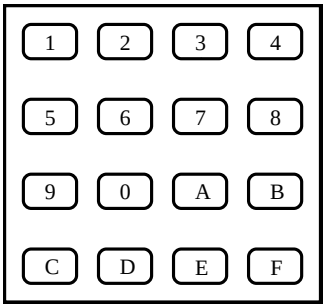


Figure 6-2 Block diagram of controller with uninterrupted mode keypad interface.

Table 6-1 Planning for I/O ports of 89C51 microcontroller.

I/O Ports	Link up
P0.0 ~ P0.7	D0 ~ D7 of LCD
P1.0	CLOCK of PLL
P1.1	DATA of PLL
P1.2	LE (Load Enable) of PLL
P1.3	LD (Lock Detect) of PLL
P1.4 ~ P1.7	Reserve
P2.0 ~ P2.3	KD0 ~ KD3 or Pin5 ~ Pin8 of keypad
P2.4 ~ P2.7	Reserve for keypad expansion or Pin1 ~ Pin4 of keypad
P3.0/RXD	E of LCD
P3.1/TXD	Reserve
P3.2/$\overline{\text{INT0}}$	$\overline{\text{INT}}$ of keypad scanning circuit
P3.3/$\overline{\text{INT1}}$	Reserve
P3.4/T0	Reserve
P3.5/T1	Reserve
P3.6/WR	R/$\overline{\text{W}}$ of LCD
P3.7/$\overline{\text{RD}}$	RS of LCD



Keypad	Functions
0 ~ 9	Numeral keys
E	Enter
B	Backspace
C	Clear

Figure 6-3 Labels and function of keypad panel.

6-1-2 Keypad and Keypad Scanning Circuit

We use a 4×4 keys keypad for our controller. The labels and functions of keypad panel are shown in figure 6-3. Interrupted mode keypad scanning signal is produced by external keypad scanning circuit. Therefore 89C51 does not need to scan the keypad frequently. When a key is being pressed, keypad scanning circuit will send an interrupted signal to 89C51 and at this time 89C51 only receives the input data from keypad. So, if no command from keypad, 89C51 can deal with other jobs such as data processing or diversity control.

Figure 6-4 is the circuit diagram of keypad scanning circuit. It is comprised by clock generator, 4-bit counter, 3-to-8 decoder, 4-to-1 multiplexer, 4-bit latch and one-shot. 4-bit counter produce scanning signal. The outputs of the lower two bits Q_0 and Q_1 are connected to the input of decoder. It is used to select one row from four rows of keypad. The truth table of keypad scanning circuit is shown in table 6-2.

If no command from keypad, then the output of every row equals one. Therefore, the output of multiplexer also equals one. Assume that keystroke “3” is been pressed, the output of counter is “1000” and the output of decoder is “1110”. Then multiplexer will select channel C2 and the output will be zero. At this moment the output terminal of one-shot will cause a

negative edge triggered signal. After one-shot is triggered, it will produce a pulse to trigger the latch, which can maintain the value of counter and send an interrupted request signal ($\overline{INT}$) to pin $\overline{INT0}$ of 89C51 microcontroller. After 89C51 accepts interrupted request, then it will read the data from latch. Therefore the procedures of input from keypad are completed.

Uninterrupted mode interface keypad scanning signal is produced by internal 89C51 microcontroller. So, this structure can determine the input from keypad without keypad scanning circuit. Therefore, it can reduce the cost of controller and the complexity of circuit. However, it will increase the length of program of controller and not easy to expand for other applications.

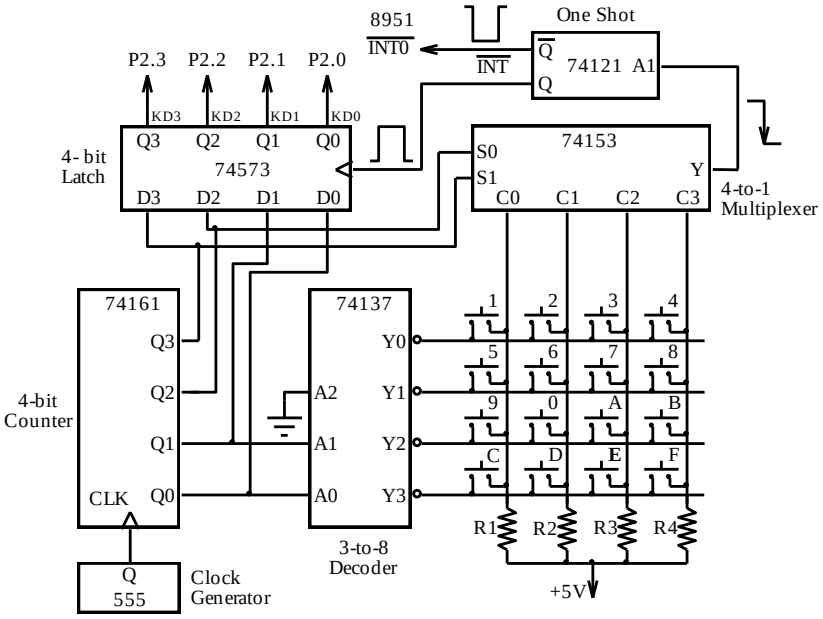


Figure 6-4 Keypad scanning circuit.

6-1-3 Liquid Crystal Display (LCD)

We use a 16 words × 2 rows characters mode LCD for our controller. This LCD includes character generator ROM (CG ROM), character generator RAM (CG RAM), display data RAM (DD RAM), busy flag (BF) and so on.

Figure 6-5 is the application circuit of LCD and table 6-2 shows the illustration of LCD

connector. The objective of VR_1 is to adjust voltage V_o which is the contrast adjustment of LCD, D7 ~ D0 connect to P0.7 ~ P0.0 of 89C51 microcontroller, RS, R/$\overline{W}$ and E are the controlled signals connecting to P3.7, P3.6 and P3.0 of 89C51 microcontroller, respectively. Table 9-4 is the instruction table of LCD. We must familiarize the commands and functions before control the LCD. Figure 6-6 is the timing figure of data in and data out for LCD. In order to write data into the register of LCD or read data from the register of LCD, we must produce timing signal by using 89C51 as shown in figure 6-6.

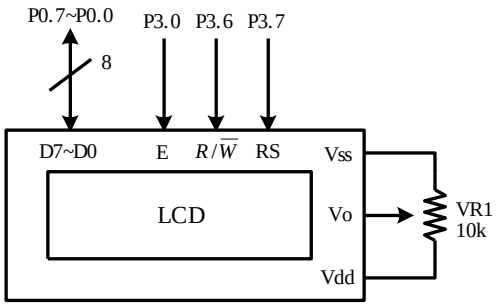
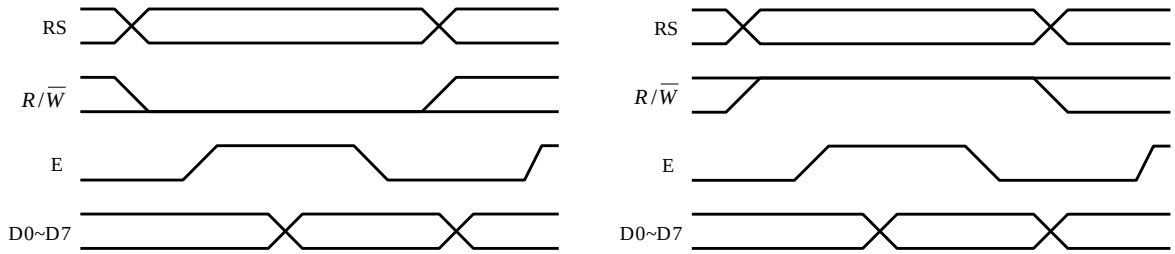


Figure 6-5 Application circuit of LCD.

Table 6-2 Illustration of LCD connector.

Connector No.	Connector Name	I/O	Functions
1	Vss	-	0 V
2	V_{DD}	-	+5 V
3	V_o	-	Contrast adjustment voltage, 0 V is the brightest for LCD
4	RS	I	Register select signal 0 : Write in command register Read from busy flag and address counter 1 : Read and write data from register
5	R/$\overline{W}$	I	0 : Write in 1 : Read from
6	E	I	Start to execute signal 1 : Read and write effective
7 ~ 14	D0 ~D7	I/O	Read or write data and commands input interface (Can operate in 4-bit or 8-bit)



(a) Data in. (b) Data out.

Figure 6-6 The timing figure of data in and data out for LCD interfaces.

6-1-4 MB 15E03L Serial Input PLL Frequency Synthesizer

MB 15E03L is a serial input PLL frequency synthesizer, which its operation frequency can reach to 1.2 GHz. MB 15E03L includes prescaler, programmable reference divider and programmable divider.

The connection interface of MB 15E03L and 89C51 microcontroller is shown in table 6-3. The output frequency of the whole PLL can be expressed as

$$f_{vco} = \left[(M \times N) + A\right] \times f_{osc} \div R \qquad (6\text{-}1)$$

where

f_{VCO} : output signal frequency of VCO.

M : divide ratio of prescaler (64 or 128).

N : divide ratio of binary 11 bits programmable counter (5 ~ 2047).

A : divide ratio of binary 7 bits swallow counter (0 ~ 127, A<N).

f_{OSC} : output frequency of the reference frequency oscillator.

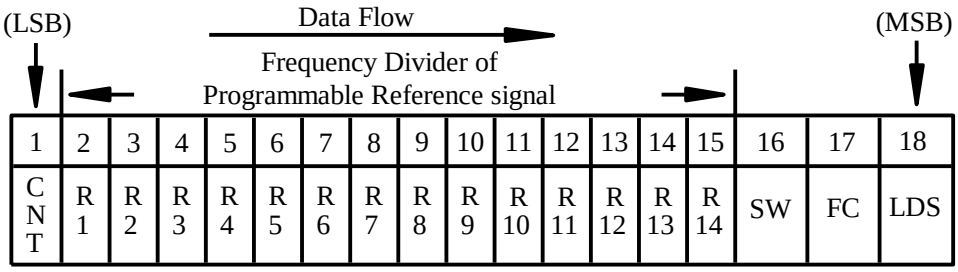
R : divide ratio of binary 14 bits programmable reference counter (5 ~ 16383).

We will discuss the calculations of each item for equation (6-1) in next chapter. Before that we discuss how the calculation values send to MB 15E03L.

Table 6-3 MB 15E03L interfaces.

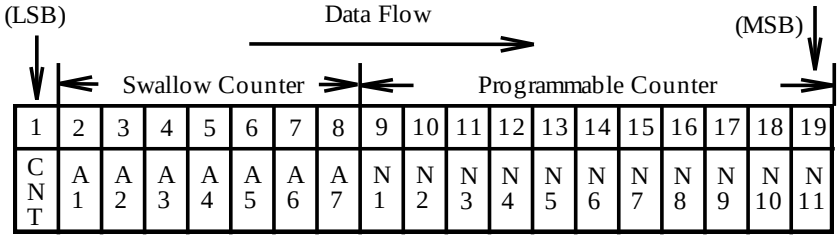
Interfaces	I/O	Functions
CLOCK	I	Provide timing for shift register
DATA	I	Binary system serial data input
LE	I	Load Enable 1 or open: Send data from shift register to latch
LD	O	Locked Detect 1: Locked 0: Unlocked

Figure 6-7 is the data format of frequency divider for programmable reference signal. R1 to R14 represent the R values for equation (6-1), altogether 14 bits that lie in between 5 to 16383. SW is to define the value of prescaler. When SW = “High”, the frequency divider of prescaler is 64. When SW = “Low”, the frequency divider of prescaler is 128. FC is the phase control bit, which defines the output status of phase comparator. For our design, we set FC = “High”. LDS is to define the output status of pin 13 of MB 15E03L. When LDS = “High”, the output of pin 13 is the phase comparator monitoring output (f_{out}). When LDS = “Low”, the output of pin 13 is the locked detector signal output (LD). For our design, we set LDS = Low. CNT is the control bit. CNT = “High” represents the data input is the data from frequency divider of programmable reference signal. CNT = “Low” represents the data input is the data from programmable divider. Figure 6-7 is the data format of frequency divider for programmable reference signal, so bit CNT should be set to High.



CNT: Control Bit
SW : Prescaler Setting Bit
FC : The Output Status Setting Bit of Phase Comparator
LDS: The Output Status Setting Bit of Pin 13 of MB15E03L

Figure 6-7 Data format of frequency divider for programmable reference signal.



CNT: Control Bit

Figure 6-8 The data format of programmable divider.

Figure 6-8 is the data format of programmable divider, which the total bits are 19. A1 to A7 represent the A values for equation (6-1), altogether 7 bits that lie in between 0 to 127. N1 to N11 represent the N values for equation (6-1), altogether 11 bits that lie in between 5 to 2047. The function of bit CNT is same as above mentioned control bit. When CNT = “High”, the data input is the data from frequency divider of programmable reference signal. When CNT = “Low”, the data input is the data from programmable divider. Therefore, in figure 6-8, bit CNT should be set to Low.

If we understand the hardware of controller, interfaces and data structures of other peripherals, then we can use program to control these peripherals and the whole circuit will operate normally.

6-2 The Processes of Software

Generally, the processes of controllers are to input a frequency from keypad and shown

the value at LCD, then convert the values to the data format of frequency synthesizer. The frequency band of the controller is started from 2250 MHz to 2350 MHz. When “2350” is inputted, the PLL output frequency is 2350 MHz and display “2350 MHz” and “LOCKED” on the LCD. On the other hand, we also use the software programming to compose the functions of the keypad as shown in table 6-4. Therefore, the controller not only can input the desirable frequency, but also can increase or decrease the output frequency of the PLL at a step value of 1 MHz or 10 MHz by the keypad “A”, “B” and “D”.

The controller that we have designed in this chapter is uninterrupted mode keypad interface. The main program flow chart is shown in figure 6-9. The program of the controller consists of five main subprograms. The discussions of each subprogram are as follow.

Table 6-4 Functions of the keypad.

Keypads	Functions
0~9	Input numeral.
Key A	±10 MHz output frequency with every press.
Key B	±1 MHz output frequency with every press.
Key C	Error deletion when the input numeral is incorrect.
Key D	Frequency controlled key, must match up with key “A” and key “B”.
Key E	Enter or input confirmation.

6-2-1 LCD Initialization

Set LCD to 8 bits data transmission, cursor switch off and display clear. Finally move the location of display to the left top corner.

6-2-2 Paging Keypad Scanning

Send a scanning signal from 89C51 and add rebound process to let users input proper

values. The function of this subprogram is to produce a corresponding data in accordance with the input of keypad. For example, when “300” is inputted, 89C51 will send “2300 MHz” serial characters to LCD for displaying and also send the corresponding data to the shift register of MB 15E03L. The situations of keying “250” to “350” are similar to the above-mentioned discussion, just the serial characters and corresponding data are different.

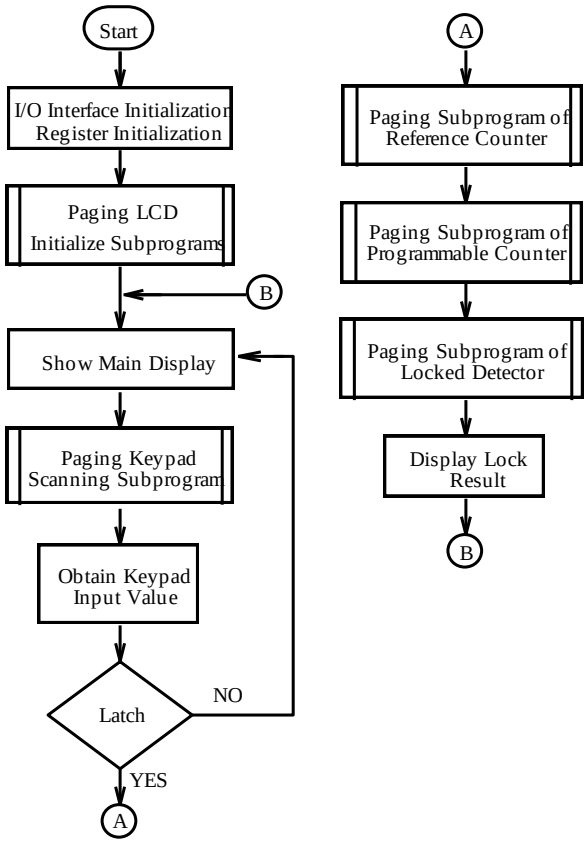


Figure 6-9 Flow chart of uninterrupted keypad interface controller.

6-2-3 Setting the Subprogram of Frequency Divider for Reference Signal

When the frequency of reference oscillator is 12 MHz and the channel space is 20 kHz, the value R of frequency divider of reference signal is equal to 300. After that add a CNT bit of control bit and SW bit of prescaler. This subprogram is to send this data to frequency divider of programmable reference signal.

6-2-4 Setting the Subprogram of Programmable Divider

The function of this subprogram is to set the output frequency of PLL from 2250 MHz to 2350 MHz. First, we must obtain the N value of programmable divider and A value of swallow counter from equation (6-1). Then add a CNT control bit and send this data to programmable divider. The corresponding values of programmable counter and swallow counter to the three frequencies are shown in table 6-5, assume that the divider (M) of prescaler be 64.

Table 6-5 Comparisons between the frequency and the values of programmable frequency divider.

Frequencies	Programmable Counter, N	Swallow Counter, A	Data of Programmable Frequency Divider
2250 MHz	1757 (6DD H)	52 (34 H)	6DD68 H
2300 MHz	1796 (704 H)	56 (38 H)	70470 H
2350 MHz	1835 (72B H)	60 (3C H)	72B78 H

6-2-5 Locked Detector

The objective of this subprogram is to detect pin LD of MB 15E03L. If LD is “High”, this means that PLL is locked, otherwise is unlocked. If PLL unlock exceeds one second, then LCD will display “UNLOCKED” and quit the program.

6-3 Design and Implementation of PLL Controller

After understanding the software and interfaces of controller, then we can design and implement the controller as shown in figure 6-10. From figure 6-10, we know that the interface between keypad and 89C51 is uninterrupted mode, i.e. 8 pins of keypad directly connect to P2.0 ~ P2.7 of 89C51. Therefore the keypad scanning signal is produced by 89C51. Then, D7 ~ D0 of LCD connect to P0.0 ~ P0.7 of 89C51. The three controlled signals RS, $R/\overline{W}$ and E connect to P3.7, P3.6 and P3.0 of 89C51, respectively. Furthermore, the data

output and input of CLK, Data, LE and LD are connected to P1.0~P1.3 of 89C51. Finally, link a 10 pins connector with MB 15E03L PLL frequency synthesizer. On the other hand, we also use resistors R_1, R_2 and variable resistor VR_1 to set the voltage at pin 3 of LCD. The objective is to control the brightness of the background of LCD.

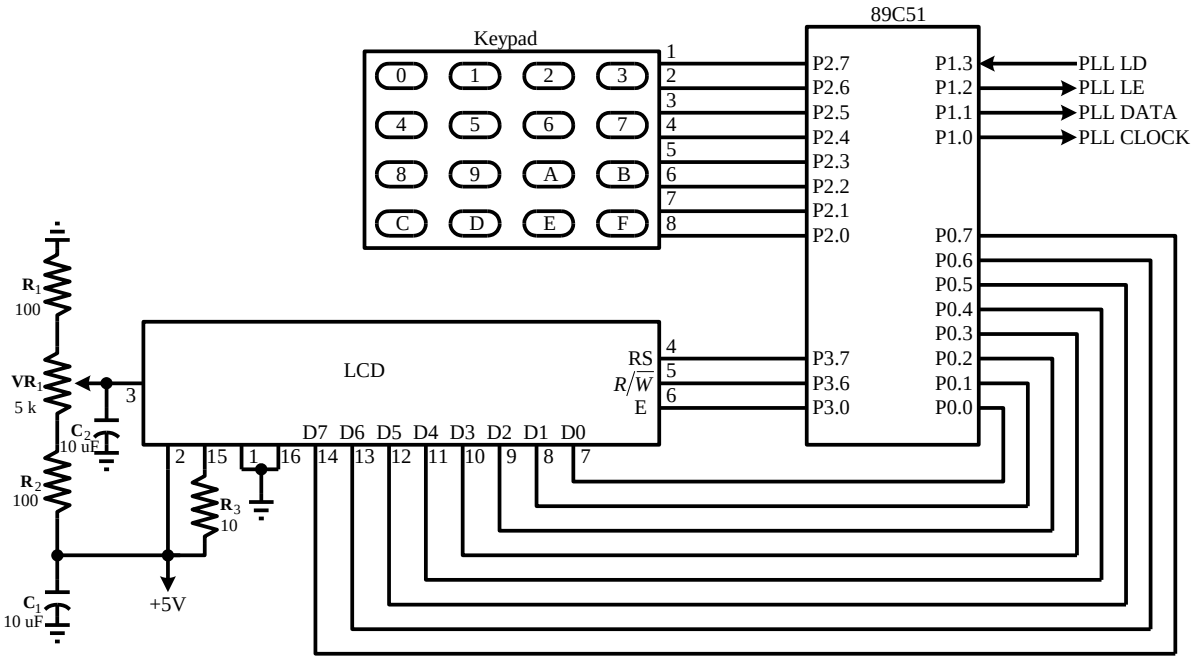


Figure 6-10 Circuit diagram of PLL controller.

III. Experiment Items

Experiment 1: LCD and keypad testing

1. To implement a PLL controller as shown in figure 6-10 or refer to figure MSA6-1 on ETEK MSA-2003-04 module.
2. Create an execute file from the program in Appendix C by 8051 compiler and link. Then program the execute file to 89C51.
3. After pressing keypad “250”, then press Enter “E”. Record the results display on LCD in table 6-6.
4. After pressing keypad “300”, then press Enter “E”. Record the results display on LCD in table 6-6.
5. After pressing keypad “A”, then record the results display on LCD in table 6-6.
6. After pressing keypad “B”, then record the results display on LCD in table 6-6.
7. After pressing keypad “D”, and then press keypad “A”. Record the results display on LCD in table 6-6.
8. After pressing keypad “D”, and then press keypad “B”. Record the results display on LCD in table 6-6.

Experiment 2: MB 15E03L control signal testing

1. To implement a PLL controller as shown in figure 6-10 or refer to figure MSA6-1 on ETEK MSA-2003-04 module.

2. Using oscilloscope to measure the signal from 89C51 to MB 15E03L. Connect the probe of CH1, CH2 and CH3 of oscilloscope to CLK, Data and LE of the connector.

3. After pressing keypad “250”, then press Enter “E”. Record the results display on LCD in table 6-7.

4. After pressing keypad “300”, then press Enter “E”. Record the results display on LCD in table 6-7.

5. After pressing keypad “A”, then record the results display on LCD in table 6-7.

6. After pressing keypad “B”, then record the results display on LCD in table 6-7.

7. After pressing keypad “D”, and then press keypad “A”. Record the results display on LCD in table 6-7.

8. After pressing keypad “D”, and then press keypad “B”. Record the results display on LCD in table 6-7.

9. From the waveforms shown in table 6-7, write down the data at the CLK positive edge triggered in binary and hexadecimal system.

IV. Experimental Results

Experiment 1: LCD and keypad testing

Table 6-6 Measured results of LCD and keypad testing.

Keypads	LCD Display
Input Key “250”	
Input Key “300”	
Input Key “A”	
Input Key “B”	
Input Key “D” and “A”	
Input Key “D” and “B”	

Experiment 2: MB 15E03L control signal testing

Table 6-7 Measured results of PLL control signal testing.

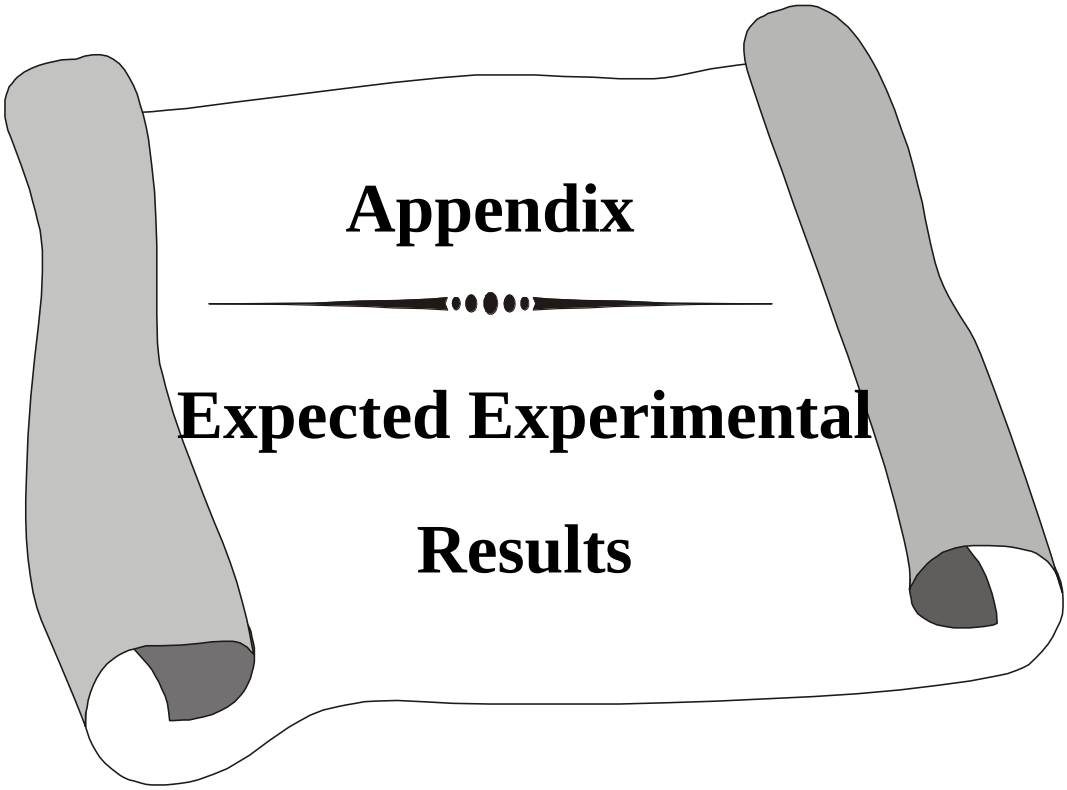
Keypad	Measurement results
Input Key “250”	Data (Binary System) =_____ Data (Hexadecimal System) =_____
Input Key “300”	Data (Binary System) =_____ Data (Hexadecimal System) =_____
Input Key “A”	Data (Binary System) =_____ Data (Hexadecimal System) =_____

Table 6-7 Measured results of PLL control signal testing (Continue).

Keypad	Measurement results
Input Key “B”	Data (Binary System) =_____ Data (Hexadecimal System) =_____
Input Key “D” and “A”	Data (Binary System) =_____ Data (Hexadecimal System) =_____
Input Key “D” and “B”	Data (Binary System) =_____ Data (Hexadecimal System) =_____

V. Problems Discussion

1. Generally, microprocessor handles the keypad signal by an interrupted mode or an uninterrupted mode. Explain the advantages and disadvantages of these two modes.
2. Describe the operation theory of interrupt mode keypad scanning circuit.
3. Describe the functions of SW bit and CNT bit when the data format of MB 15E03L is the programmable reference signal divider.
4. Describe the functions of FC bit and LDS bit when the data format of MB 15E03L is the programmable reference signal divider.
5. List the five subprograms in the programming of the controller and also describe the functions of each subprogram.
6. If the R value of programmable reference signal divider is equal to 320 and the M value of prescaler is equal to 128, then find the data, which send to programmable reference signal divider from 89C51. (binary system and hexadecimal system)
7. If the N value of programmable counter is equal to 507 and the A value of remainder counter is equal to 64, then find the data, which send to programmable divider from 89C51? (binary system and hexadecimal system)



Appendix

Expected Experimental Results

Chapter 6: Phase Locked Loop Controller

Experiment 1: LCD and keypad testing

Table 6-6 Measured results of LCD and keypad testing.

Keypads	LCD Display
Input Key “250”	BAND RF=2250 MHz LOCKED!!
Input Key “300”	BAND RF=2300 MHz LOCKED!!
Input Key “A”	BAND RF=2310 MHz LOCKED!!
Input Key “B”	BAND RF=2311 MHz LOCKED!!
Input Key “D” and “A”	BAND RF=2301 MHz LOCKED!!
Input Key “D” and “B”	BAND RF=2300 MHz LOCKED!!

Experiment 2: MB 15E03L control signal testing

Table 6-7 Measured results of PLL control signal testing.

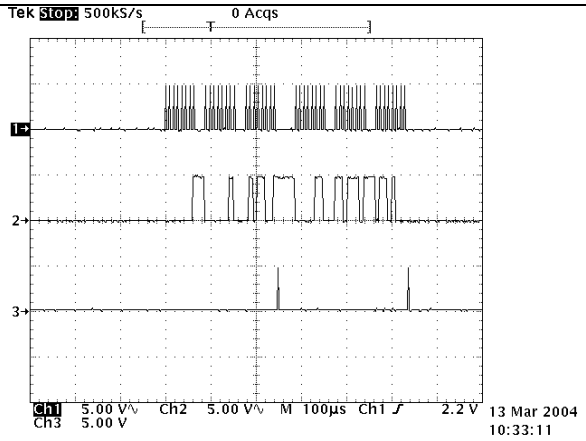
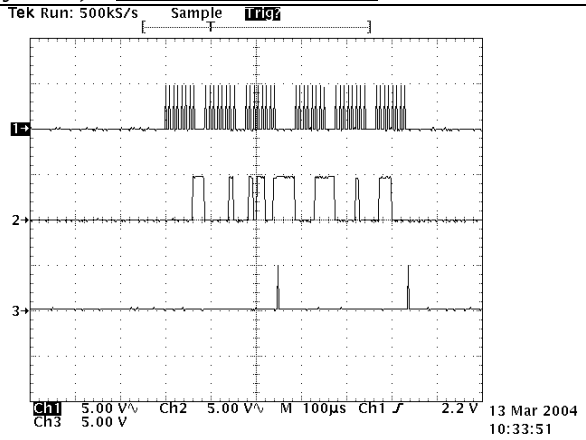
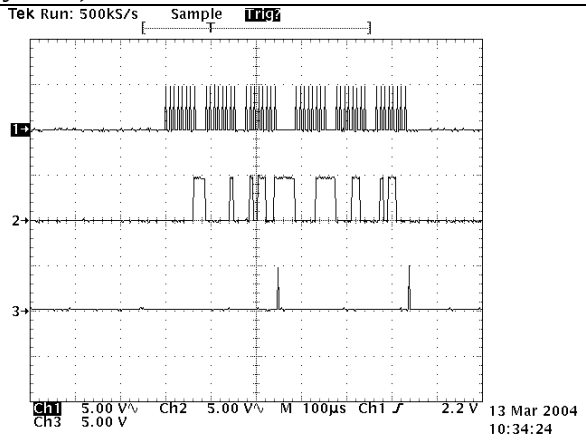
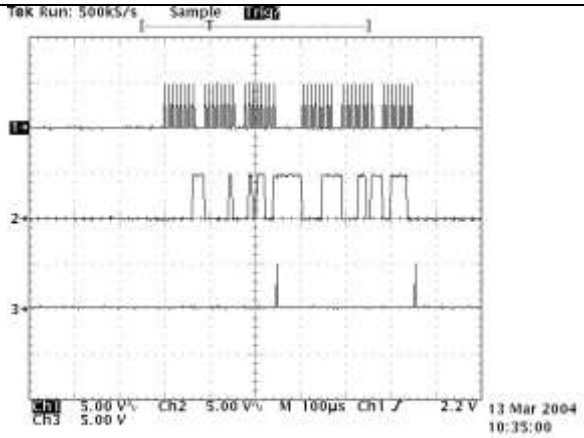
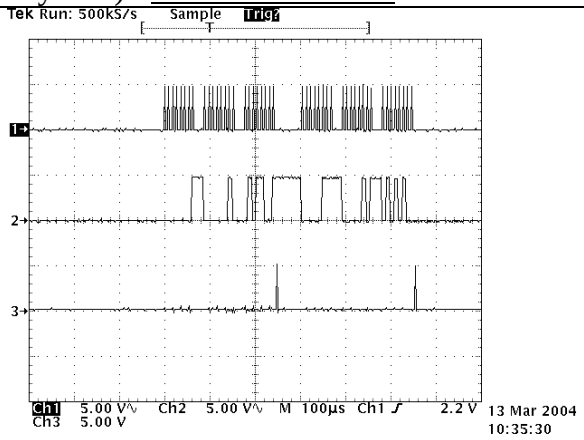
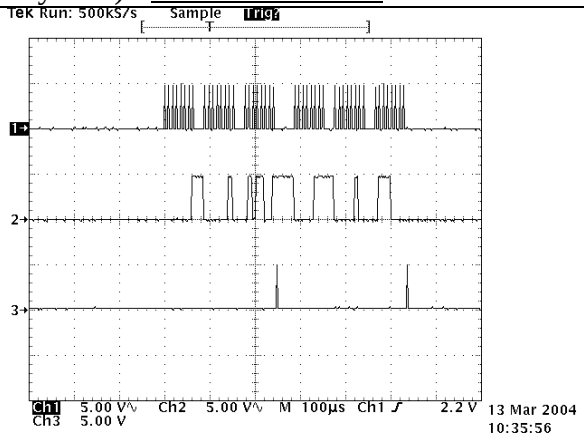
Keypad	Measurement results
Input Key “250”	 Data(Binary System) = 00000001 00000010 01011001 00000110 11011101 01101000 Data(Hexadecimal System) = 01025906DD68 H
Input Key “300”	 Data(Binary System) = 00000001 00000010 01011001 00000111 00000100 01110000 Data(Hexadecimal System) = 010259070470 H
Input Key “A”	 Data(Binary System) = 00000001 00000010 01011001 00000111 00001100 01011000 Data(Hexadecimal System) = 010259070C58 H

Table 6-7 Measured results of PLL control signal testing (Continue).

Keypad	Measurement results
Input Key "B"	 Data(Binary System) = 00000001 00000010 01011001 00000111 00001101 00111100 Data(Hexadecimal System) = 010259070D5C H
Input Key "D" and "A"	 Data(Binary System) = 00000001 00000010 01011001 00000111 00000101 01010100 Data(Hexadecimal System) = 010259070554 H
Input Key "D" and "B"	 Data(Binary System) = 00000001 00000010 01011001 00000111 00000100 01110000 Data(Hexadecimal System) = 010259070470 H