Trainer Module: ETEK HCS-8000-02

Chapter Three

QPSK Modulator

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I. Curriculum Objectives

1. To understand the operation theory of the bit splitter.
2. To understand the operation theory of the balanced modulator.
3. To design the balanced modulator by using MC1496.
4. To understand the methods of measuring and adjusting the balanced modulator circuit.

II. Curriculum Theory

In the communication systems, besides PSK modulation that we have mentioned before, there is another type of modulation, which we called quadrature phase shift keying (QPSK) modulation. Both PSK and QPSK modulations use the variation of phase of the carrier to modulate the data signal. However, the main difference between PSK and QPSK modulations is PSK modulation uses binary system, which means the phase difference of the carrier signal is 180° that represents “1” or “0” for the data signal. If the data signal is not binary system, but M-ary level, then we can use QPSK, 8PSK and so on to transmit the data signal more effectively. These types of modulations just use the phase shift within 360° to represent the M-ary levels. Therefore, N-bits of data signal can be transmitted at the same time. This will reduce the transmitted bandwidth and a high transmission rate can be achieved.

QPSK modulated signal is a system with M = 4 levels, which means 2 bits data will be transmitted at the same time. From the equation (3-1), we know that the QPSK modulated signal can be expressed as

$$x_{QPSK}(t) = A\cos\left[\omega_c t + (2m-1)\frac{\pi}{4}\right];\ m = 1, 2, 3, 4 \qquad (3\text{-}1)$$

From the above equation, we know that the phase of carrier of the QPSK modulated signal is distributed to $\pi/4$, $3\pi/4$, $5\pi/4$ and $7\pi/4$. Each phase represents 2 bits data signal as shown in table 3-1. The signal constellation diagram is shown in figure 3-1.

Expanding equation (3-1), we get

$$x_{QPSK}(t) = A\cos[(2m-1)\frac{\pi}{4}]\cos(\omega_c t) - A\sin[(2m-1)\frac{\pi}{4}]\sin(\omega_c t) \quad (3\text{-}2)$$

Table 3-1 The signal constellation characteristics of quadrature phase shift keying.

Phases of QPSK	2 bits inputs
$\pi/4$	11
$3\pi/4$	10
$5\pi/4$	00
$7\pi/4$	01

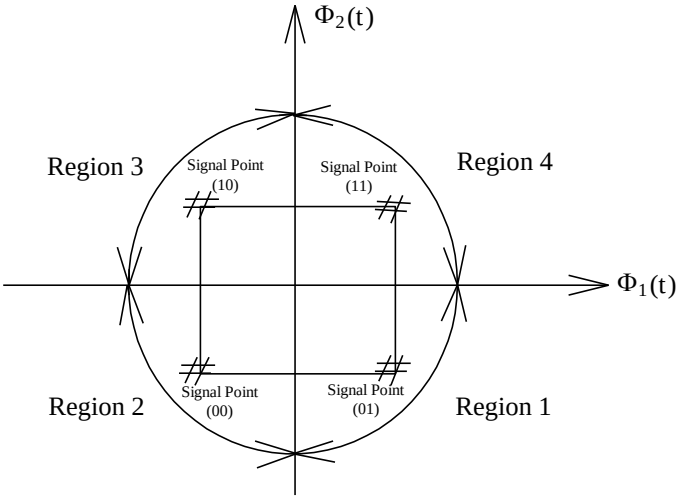


Figure 3-1 The signal constellation diagram of QPSK modulation.

From equation (3-2), it exits a group of orthogonal functions, which are

$$\Phi_1(t) = A\cos(\omega_c t) \tag{3-3a}$$

$$\Phi_2(t) = A\sin(\omega_c t) \tag{3-3b}$$

So, from equation (3-1), QPSK modulated signal can be simplified as

$$x_{QPSK}(t) = \cos[(2m-1)\frac{\pi}{4}]\cdot\Phi_1 - \sin[(2m-1)\frac{\pi}{4}]\cdot\Phi_2 \tag{3-4}$$

From the above equation, QPSK modulated signal can be assumed as a combination of two BPSK modulation signal.

Figure 3-2 is the basic block diagram of the QPSK modulator. From the block diagram, the input data signal has to be converted to parallel output by the multiplexer. The outputs of the multiplexer are the I-data and Q-data, which will match with the orthogonal functions and the balanced modulators to obtain the I-data of BPSK modulation signal (I-BPSK) and Q-data of BPSK modulation signal (Q-BPSK). These two groups of data will be summed to produce the QPSK modulated signal.

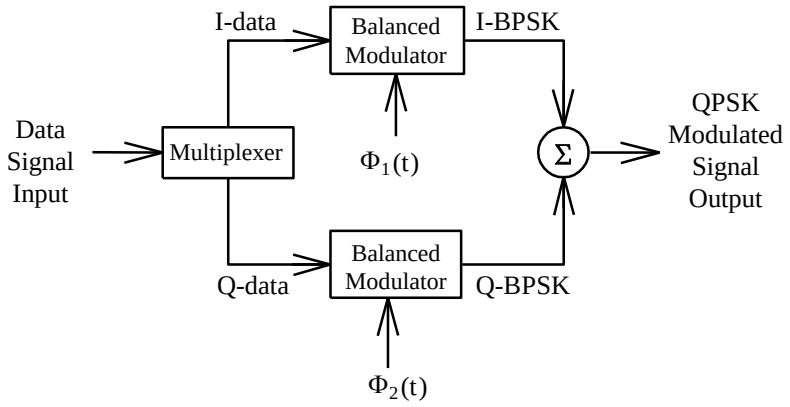


Figure 3-2 The basic block diagram of QPSK modulator

Figure 3-3 shows the circuit block diagram of QPSK modulator. 2 bits data (2 bits in a group) is sent to the bit splitter at the same time. These two groups of data will be split to parallel data. One of them will lead to I channel to become I-data and the other will lead to Q channel to become Q-data. The phase of I-data is similar to the carrier of the reference oscillator, which will be modulated to become I-BPSK. However, the phase difference between Q-data and the carrier of the reference oscillator is 90°, which will be modulated to become Q-BPSK. We know that the QPSK modulator is the combination of two BPSK modulators. Thus, at the output terminal of the I balanced modulator (I-BPSK), there are two types of phases will be produced, which are $+\cos\omega_c t$ and $-\cos\omega_c t$. Similarly, at the output terminal of the Q balanced modulator (Q-BPSK), there are also two types of phases will be produced, which are $+\sin\omega_c t$ and $-\sin\omega_c t$. When the summer combines these two groups of orthogonal BPSK modulated signal, there will be four possible phases which are $+\sin\omega_c t+\cos\omega_c t$, $+\sin\omega_c t-\cos\omega_c t$, $-\sin\omega_c t+\cos\omega_c t$ and $-\sin\omega_c t-\cos\omega_c t$.

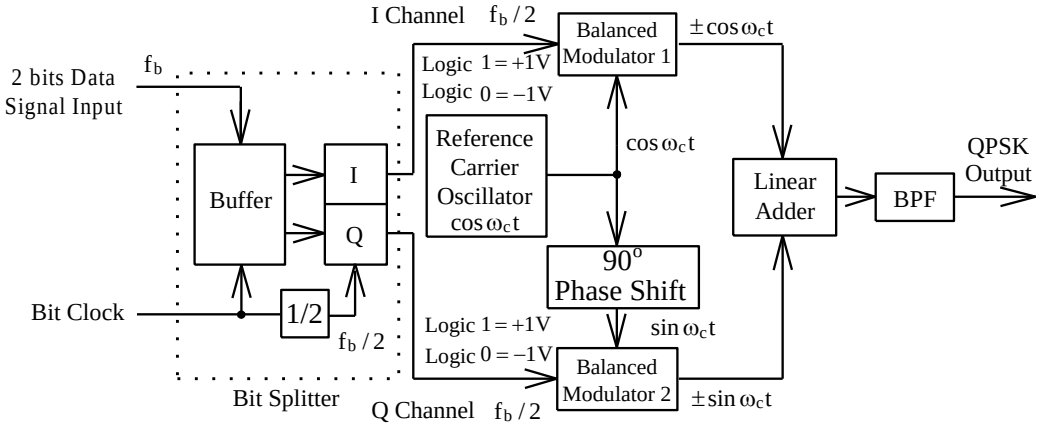
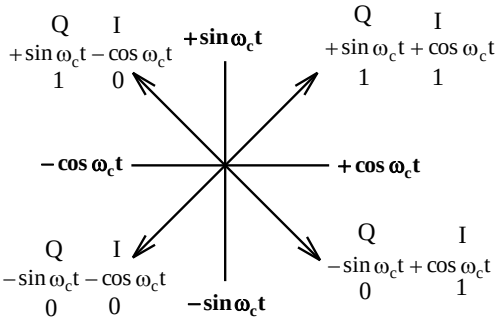


Figure 3-3 The circuit block diagram of QPSK modulator.

Figure 3-4(a) is the truth table of the phase output of QPSK modulation and figure 3-4(b) is the constellation diagram of QPSK modulation. From figure 3-4 (b), QPSK has four possible signal constellations with same amplitude and the phase difference is 90^o. Therefore, although the QPSK signal has a $\pm 45^o$ deviation during transmission, the receiver still can demodulate the signal correctly.

Figure 3-5 to figure 3-10 are the details circuit diagrams of each block of QPSK modulator in figure 3-3. Figure 3-5 is the circuit diagram of pseudo random data generator. It is comprised by BCD counter and logic gates. By using the characteristics of frequency division of the asynchronous counter, the input CLK signal will be divided by 3 and the output signal can be obtained from Q_1, which is a pseudo random data signal. The function of AND gate is to ensure that the counter achieved the motion of division 3. When the output of counter Q_0 and Q_1 are 1, then the counter will reset to the original value.

Binary Input		Phase Output of QPSK Modulation Signal
Q	I	
0	0	-135^o
0	1	-45^o
1	0	$+135^o$
1	1	$+45^o$



(a) The truth table of phase output (b) The constellation diagram

Figure 3-4 The truth table and the constellation diagram of QPSK modulator

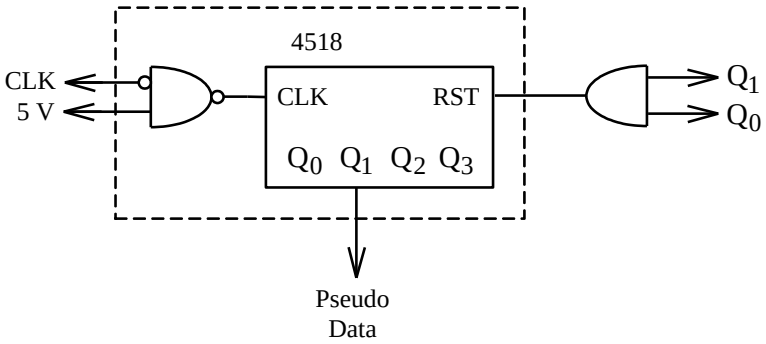


Figure 3-5 The circuit diagram of pseudo random data generator.

Figure 3-6 shows the bit splitter, which is comprised by four D-flip flops and one JK flip flop. D-flip flop 1 (DFF1) and D-flip flop 2 (DFF2) comprise a shift register, which its transmission rate is the same as the data rate. JK flip flop 1 (JKFF1) and XOR gate comprise an inverter. The objective is to invert the CLK signal, then it will pass through the capacitor to delay the signal so that the D-flip flop 3 (DFF3) and D-flip flop 4 (DFF4) are able to convert the serial input to parallel output, which are I-data and Q-data. The duty cycle of I-data and Q-data are the double the original data signal, $2T_b$.

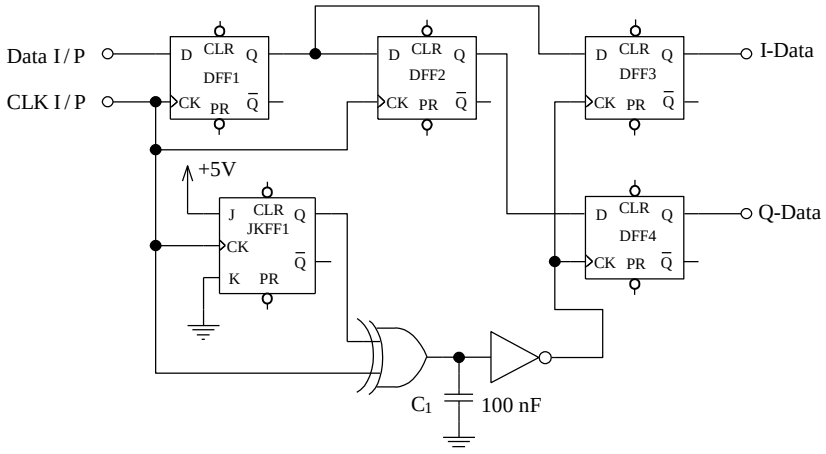


Figure 3-6 Bit splitter.

Figure 3-7 shows the unipolar to bipolar converter, which is comprised by 74HCU04, 74HC126, 3904, 3906, D_{Z1}, D_{Z2}, D_{Z3} and R_1 to R_8. The objective of this circuit is to convert the unipolar I-data and unipolar Q-data to bipolar I-data and bipolar Q-data. After that these signals will be inputted to pin 1 of MC1496. The operation theory is to invert the digital signal by inverter (74HCU04) and then pass through two followers (74HC126) to split the signal into two. These two signals will pass through the switch, which is comprised by 3904, 3906, D_{Z1}, D_{Z2}, D_{Z3} and R_1 to R_8 to convert the unipolar signal to bipolar signal.

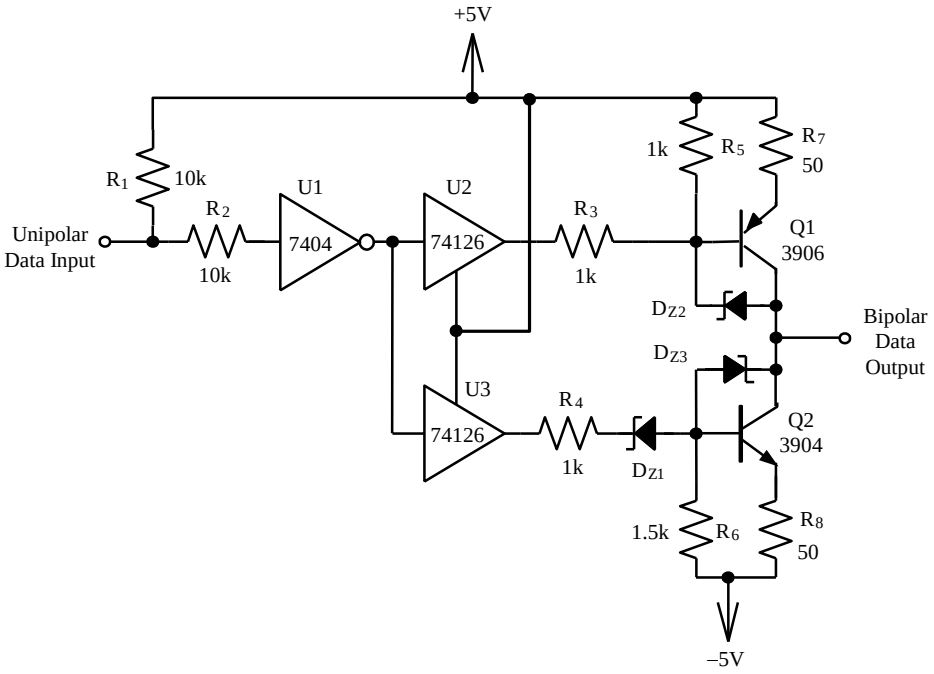


Figure 3-7 The circuit diagram of unipolar to bipolar converter.

Figure 3-8 shows the details circuit diagram of balanced modulator. The balanced modulator is comprised by MC1496. Both the carrier signal and data signal are single-ended inputs. The carrier signal is inputted at pin 10 and the data signal is inputted at pin 1. The R_{13} and R_{14} determine the gain and the bias current of the circuit, respectively. If we adjust VR_1 or the amplitude of digital signal, we may prevent the modulated signal from distortion. Then this signal will pass through the filter, which is comprised by μA741, C_3, C_5, R_{17}, R_{18} and R_{19}. The objective is to remove the high frequency signal in order to obtain the optimum PSK signal.

Figure 3-9 shows the phase shifter, which is used to shift the phase of carrier signal. This situation will produce a group of orthogonal carrier signal, which will supply to the balanced modulators of I-channel and Q-channel. The phase angle (θ) is related to R_i, C_i and the frequency of carrier. The expression is

$$R_i = \frac{\tan(\frac{\theta}{2})}{2\pi f C_i} \qquad (3\text{-}5)$$

Figure 3-10 shows the circuit diagram of linear summer. The objective of the linear summer is to combine the two groups of the orthogonal BPSK modulation signals to become a QPSK signal.

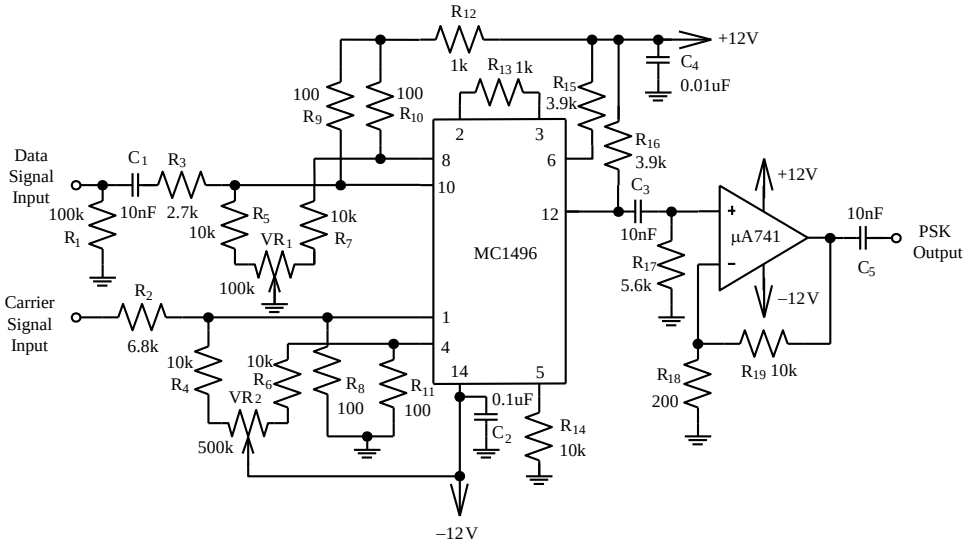


Figure 3-8 The circuit diagram of balanced modulator.

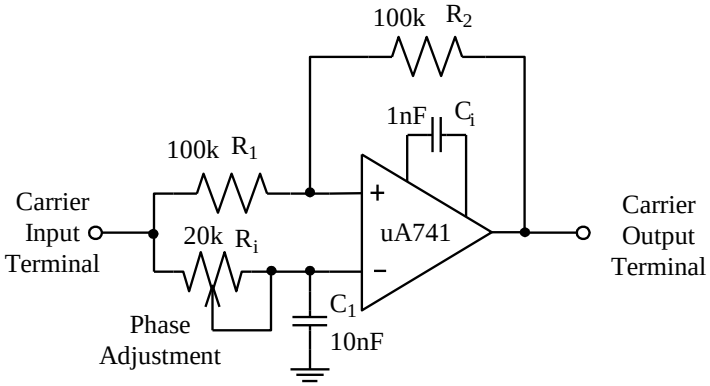


Figure 3-9 The circuit diagram of phase shifter.

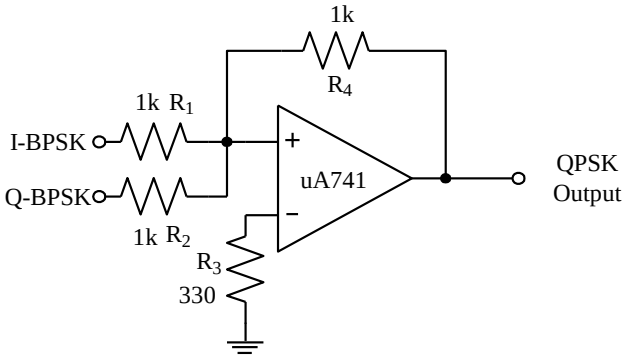


Figure 3-10 The circuit diagram of linear summer.

III. Experiment Items

Experiment 1: Bit splitter

1. To implement the bit splitter as shown in figure 3-6 or refer to figure 3-1 on ETEK HCS-8000-02 module.

2. At input terminal of CLK signal (CLK I/P), input 5 V amplitude, 300 Hz frequency TTL waveform and the duty cycle is 50 %.

3. By using oscilloscope, observe on the Pseudo random data output terminal (Pseudo Data), I-Data output terminal and Q-Data output terminal of bit splitter, then record the measured results in table 3-2.

4. According to the input signals in table 3-2, repeat step 3 and record the measured results in table 3-2.

Experiment 2: QPSK modulator

1. To implement the QPSK modulator as shown in figure 3-3 or refer to figure 3-1 on ETEK HCS-8000-02 module.

2. At input terminal of CLK signal (CLK I/P), input 5 V amplitude, 300 Hz frequency TTL waveform and the duty cycle is 50 %.

3. By using oscilloscope, observe on the Pseudo random data output terminal (Pseudo Data), I-Data output terminal of bit splitter, Q-Data output terminal of bit splitter, output terminals (TP1 and TP2) of unipolar to bipolar converter, then record the measured results in table 3-3.

4. According to the input signals in table 3-3, repeat step 3 and record the measured results in table 3-3.

5. At the carrier signal input terminal (Carrier I/P), input a 3.6 V amplitude and 20 kHz sine wave frequency.

6. By using oscilloscope, observe on the output terminals of I-Carrier and Q-Carrier of phase shifter, then adjust the variable resistor (Phase Adjust), so that the phase difference between I-Carrier and Q-Carrier is 90°, then record the measured results in table 3-4.

7. By using oscilloscope, observe on the signal output terminal of balanced modulator 1 (TP3), adjust variable resistor (I-Carrier Adjust), until the waveform without occurring distortion. Then slightly adjust variable resistor (I-Data Adjust) to avoid the asymmetry of the waveform. Finally record the output signal waveform of the balanced modulator in table 3-4, which is the I-BPSK modulated signal.

8. By using oscilloscope, observe on the signal output terminal of balanced modulator 2 (TP4), adjust variable resistor (Q-Carrier Adjust), until the waveform without occurring distortion. Then slightly adjust variable resistor (Q-Data Adjust) to avoid the asymmetry of the waveform. Finally record the output signal waveform of the balanced modulator in table 3-4, which is the Q-BPSK modulated signal.

9. By using oscilloscope, observe on the output terminal of linear summer, which is the combination of I-BPSK and Q-BPSK modulation signals. Then record the measured results in table 3-4, which is the QPSK modulated signal.

10. According to the input signals in table 3-4, repeat step 7 to step 9 and record the measured results in table 3-4.

IV. Experimental Results

Table 3-2 The measured results of bit splitter by changing the frequency of data signal.

CLK Signal Frequency	300 Hz	1 kHz
Pseudo Random Data Output Terminal		
I-Data Output Terminal of Bit Splitter		
Q-Data Output Terminal of Bit Splitter		

Table 3-3 The measured results of QPSK modulator by changing the frequency of data signal. (V_C = 3.6 V_{PP}, f_C = 20 kHz)

CLK Signal Frequency	300 Hz	1 kHz
Pseudo Random Data Output Terminal		
I-Data Output Terminal of Bit Splitter		
Q-Data Output Terminal of Bit Splitter		

Table 3-3 The measured results of QPSK modulator by changing the frequency of data signal. (V_C = 3.6 V_{PP}, f_C = 20 kHz) (Continue)

CLK Signal Frequency	300 Hz	1 kHz
Output Terminals (TP1) of unipolar to bipolar converter (I-Data)		
Output Terminals (TP2) of unipolar to bipolar converter (Q-Data)		

Table 3-4 The measured results of QPSK modulator by changing the frequency of data signal. (V_C = 3.6 V_{PP}, f_C = 20 kHz)

CLK Signal Frequency	300 Hz	1 kHz
I-Carrier of Phase Shifter		
Q-Carrier of Phase Shifter		
Balanced Modulator 1 (TP3) (I-BPSK)		

Table 3-4 The measured results of QPSK modulator by changing the frequency of data signal. (V_C = 3.6 V_{PP}, f_C = 20 kHz) (Continue)

CLK Signal Frequency	300 Hz	1 kHz
Balanced Modulator 2 (TP4) (Q-BPSK)		
Output Terminal of Linear Summer (QPSK O/P)		

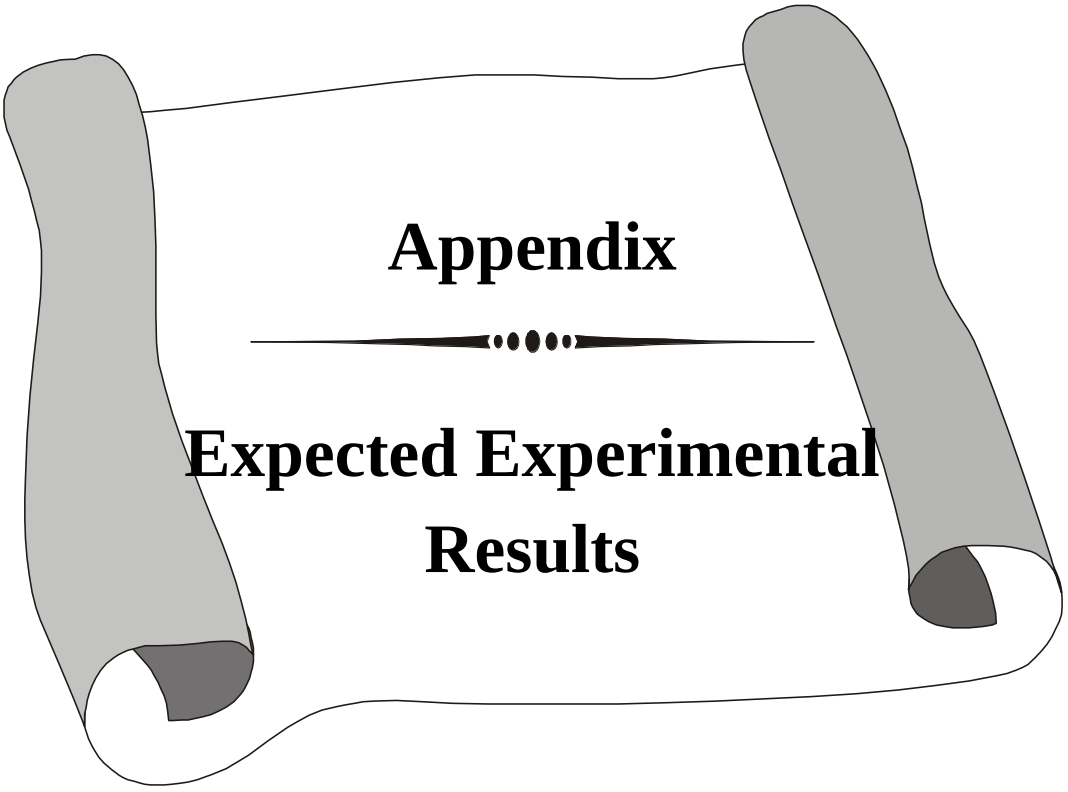
V. Problems Discussion

1. What are the basic circuit structures of QPSK modulator and also explain its operation theory?

2. What is the operation theory of bit splitter?

3. If the data input of bit splitter is 50% duty cycle, what are the output signals of I-Data output terminal and Q-Data output terminal of bit splitter?

4. If we need the input phase and output phase to be 90° phase difference, then what are the values for R_i and C_i as shown in figure 3-9? (Assume the carrier frequency is 100 kHz)



Appendix

Expected Experimental Results

Chapter 3: QPSK Modulator

Table 3-2 The measured results of bit splitter by changing the frequency of data signal.

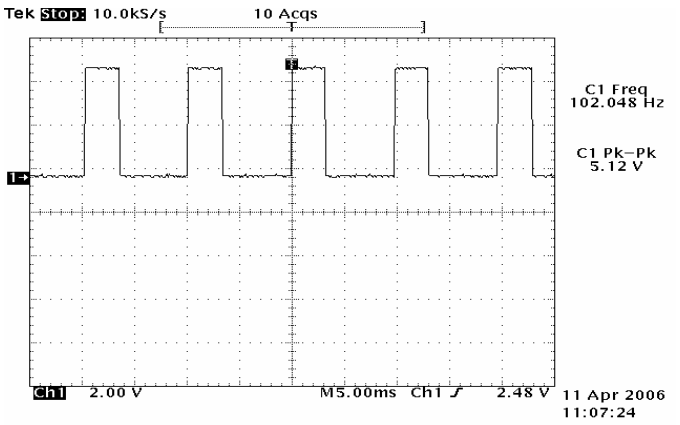
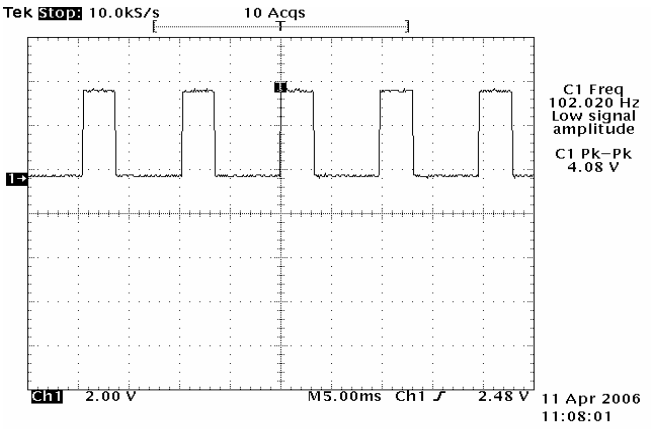
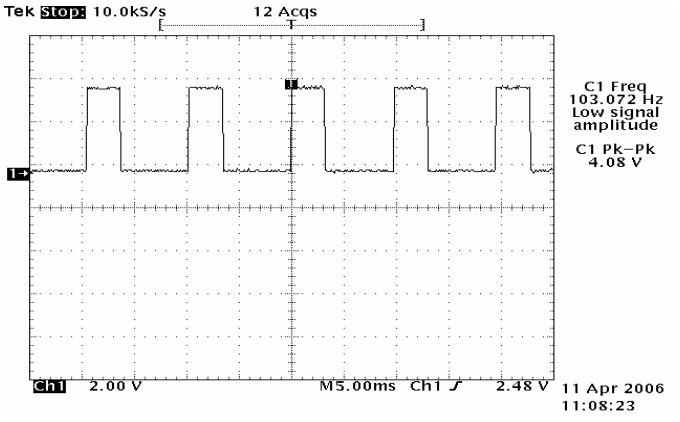
CLK Signal Frequency	300 Hz
Pseudo Random Data Output Terminal	
I-Data Output Terminal of Bit Splitter	
Q-Data Output Terminal of Bit Splitter	

Table 3-3 The measured results of QPSK modulator by changing the frequency of data signal. (V_C = 3.6 V_{PP}, f_C = 20 kHz)

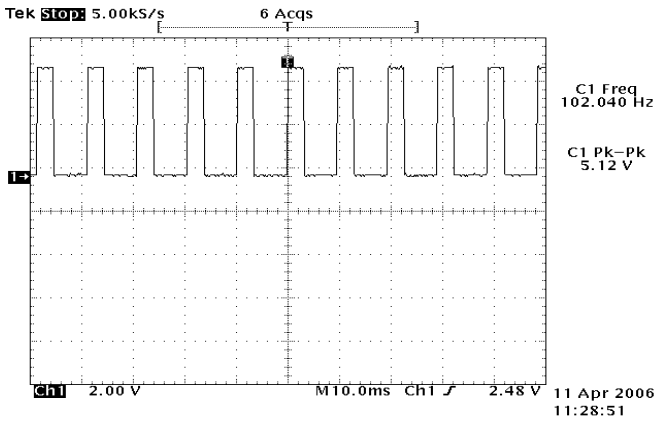
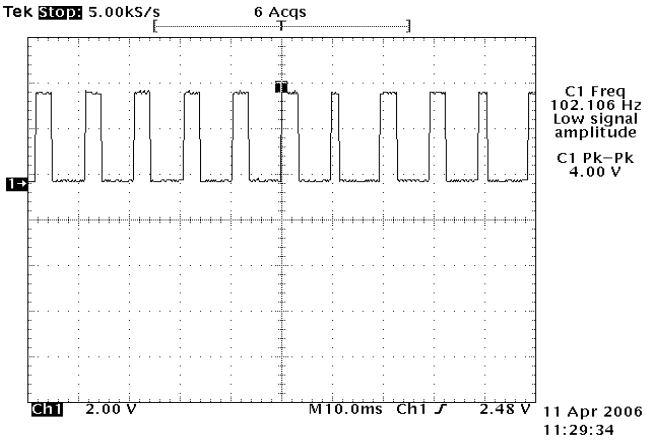
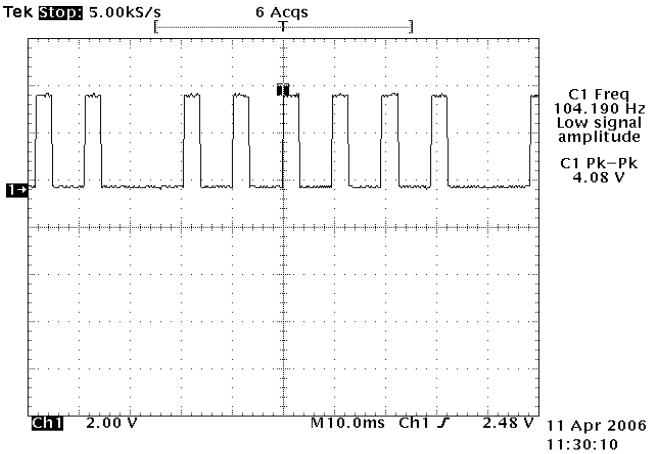
CLK Signal Frequency	300 Hz
Pseudo Random Data Output Terminal	
I-Data Output Terminal of Bit Splitter	
Q-Data Output Terminal of Bit Splitter	

Table 3-3 The measured results of QPSK modulator by changing the frequency of data signal. (V_C = 3.6 V_{PP}, f_C = 20 kHz) (Continue)

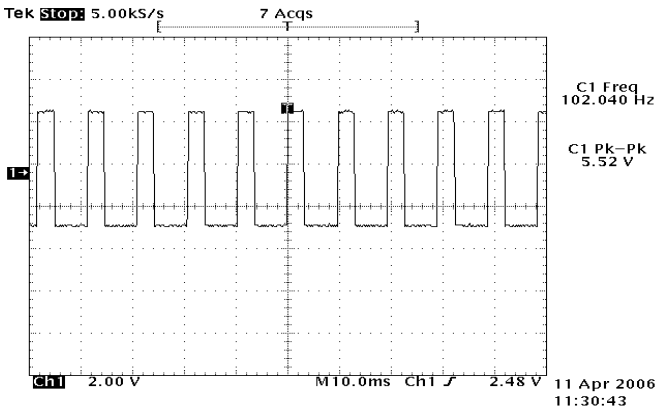
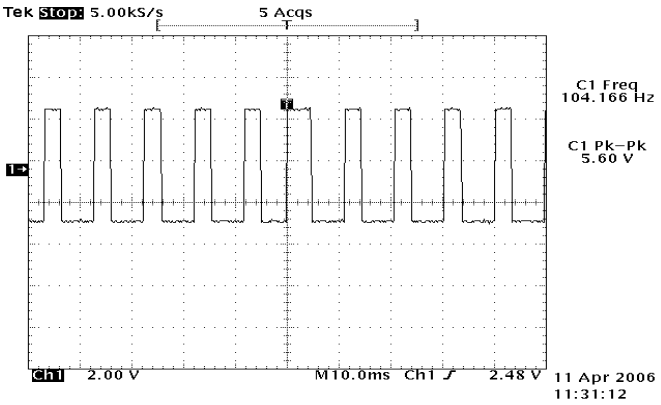
CLK Signal Frequency	300 Hz
Output Terminals (TP1) of unipolar to bipolar converter (I-Data)	
Output Terminals (TP2) of unipolar to bipolar converter (Q-Data)	

Table 3-4 The measured results of QPSK modulator by changing the frequency of data signal. (V_C = 3.6 V_{PP}, f_C = 20 kHz)

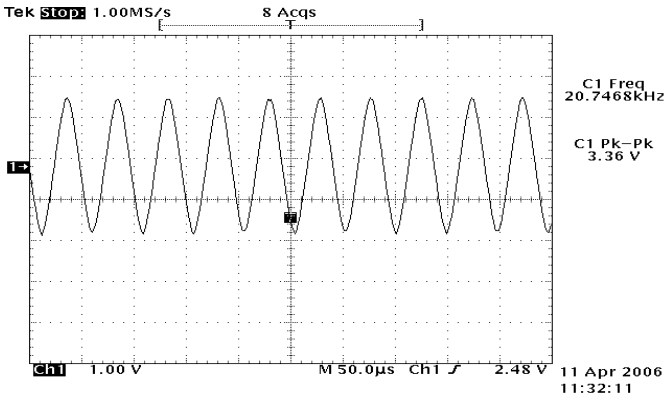
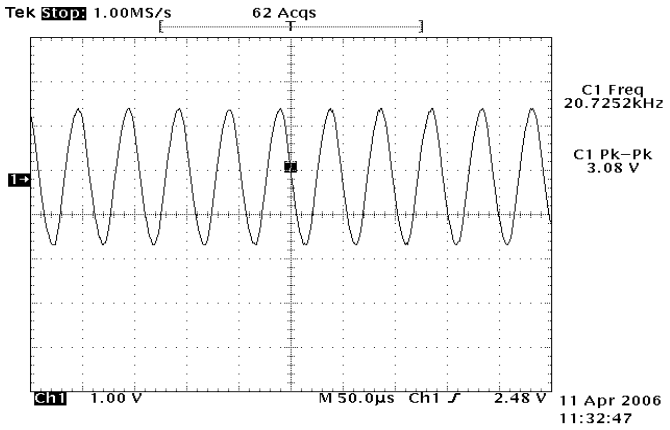
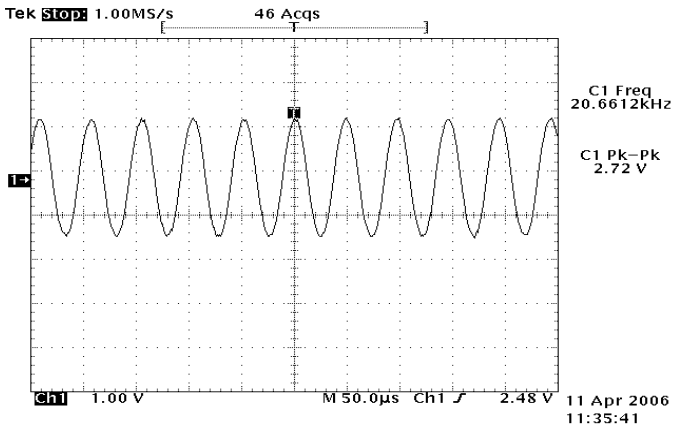
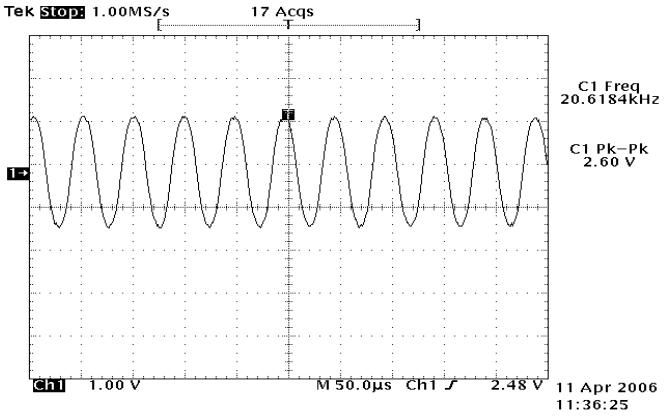
CLK Signal Frequency	300 Hz
I-Carrier of Phase Shifter	
Q-Carrier of Phase Shifter	
Balanced Modulator 1 (TP3) (I-BPSK)	

Table 3-4 The measured results of QPSK modulator by changing the frequency of data signal. (V_C = 3.6 V_{PP}, f_C = 20 kHz) (Continue)

CLK Signal Frequency	300 Hz
Balanced Modulator 2 (TP4) (Q-BPSK)	
Output Terminal of Linear Summer (QPSK O/P)